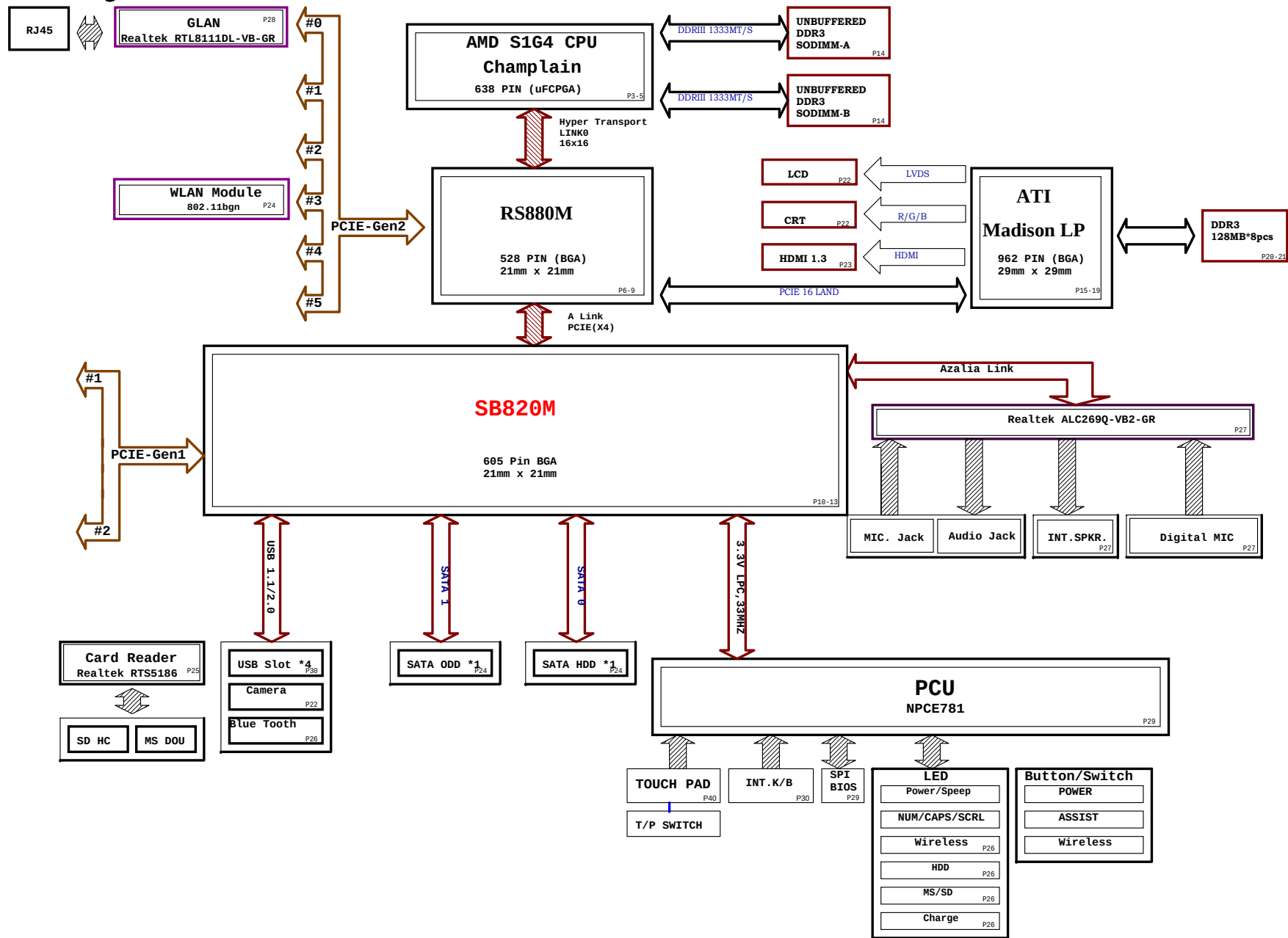
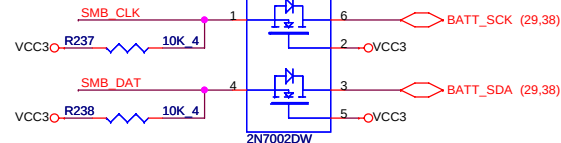
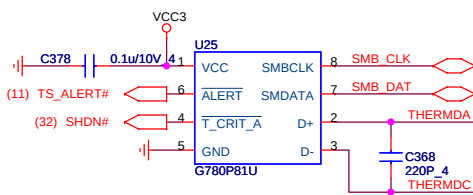
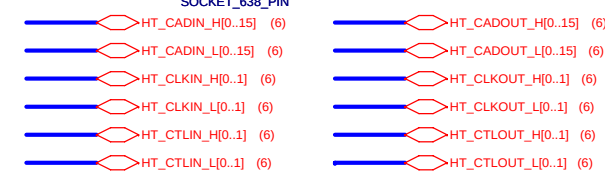
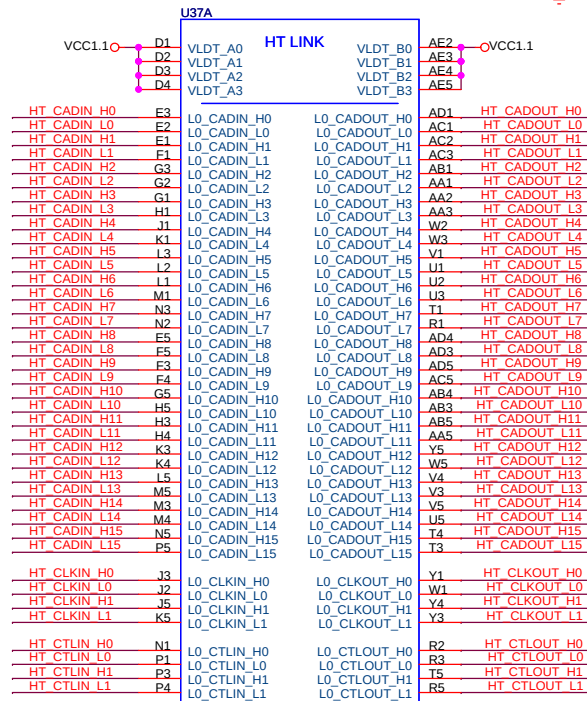
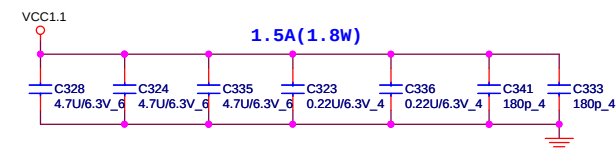


Page	Title of schematic page	Rev.	Date
01	Page List	2A	12/24
02	Block Diagram	2A	12/24
03	CPU-Champlain HT/CONTROL (1/3)	2A	01/04
04	CPU-Champlain MEMORY (2/3)	1B	12/16
05	CPU-Champlain POWER/GND (3/3)	1B	12/08
06	NB-RS880M HT/SP-MEM (1/4)	1B	12/08
07	NB-RS880M GFX/PCIE (2/4)	1A	09/24
08	NB-RS880M SYSTEM (3/4)	1A	09/24
09	NB-RS880M POWER (4/4)	1A	09/24
10	SB-SB820M PCI/CLK/LPC (1/4)	1A	09/24
11	SB-SB820M AUDIO/USB (2/4)	1A	09/24
12	SB-SB820M SATA (3/4)	1B	12/08
13	SB-SB820M POWER (4/4)	1A	09/24
14	DDR3 SODIMM* 2 (5.2mm+9.2mm)	2A	12/24
15	ATI-Madison LP PCIE/LVDS (1/5)	2A	12/24
16	ATI-Madison LP MAIN I/O (2/5)	2A	12/24
17	ATI-Madison LP POWER/GND (3/5)	2A	12/24
18	ATI-Madison LP Display POWER (4/5)	2A	12/24
19	ATI-Madison LP MEM I/F (5/5)	2A	12/24
20	ATI-Madison LP (DDR3 V-ram a)	2A	12/24
21	ATI-Madison LP (DDR3 V-ram b)	1B	12/08
22	CRT/LVDS	2A	12/24

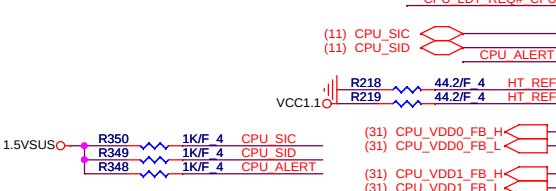
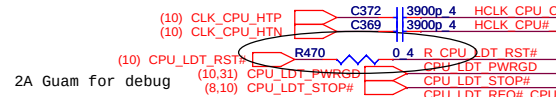
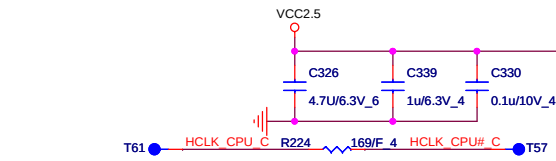
Page	Title of schematic page	Rev.	Date
23	HDMI	1B	12/09
24	WLAN/HDD/ODD	1B	12/08
25	Card Reader RTS5186	1B	12/08
26	Express Card/BT/LED	1B	12/08
27	Codec-ALC269Q VB5 GR	1B	12/08
28	LAN RTL8111E	1B	12/08
29	NPCE781	1B	12/08
30	KB/USB/FAN/PS	1B	12/09
31	VCORE(ISL6265A)	1A	09/24
32	3VPCU&5VPCU(PM6686)	1A	09/24
33	1.5VSUS/VTT_MEM	1A	09/24
34	DYN_VCC1.1(OZ8116LN)	1A	09/24
35	VCC1.1(OZ8116LN)-7A	1A	09/24
36	VGA_CORE(OZ8116)-16A	1A	09/24
37	VCC1.8/0.9/2.5/1.0	1A	09/24
38	POWER(BAT IN / ADA IN/ UL)	1A	09/24
39	CHARGER (ISL6252A)	1A	09/24
40	Small board connector	1A	09/24
41	Power Sequence		
42	CHANGE LIST		

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

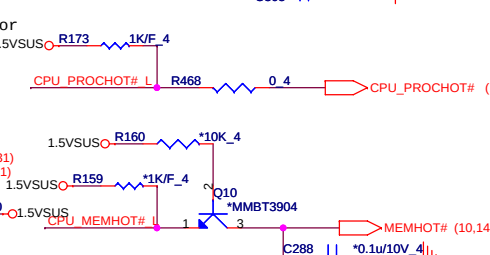
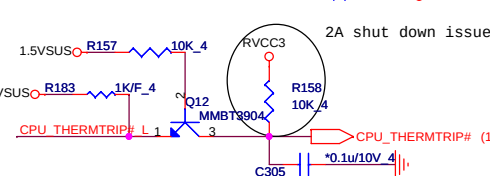
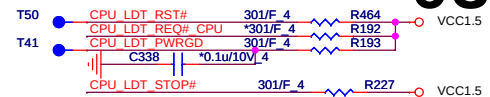
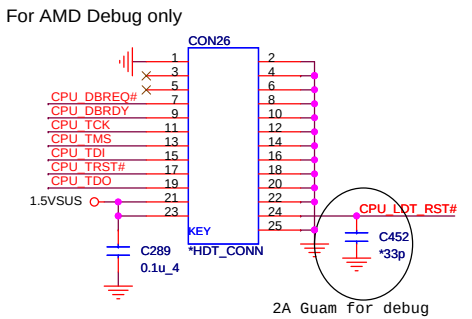
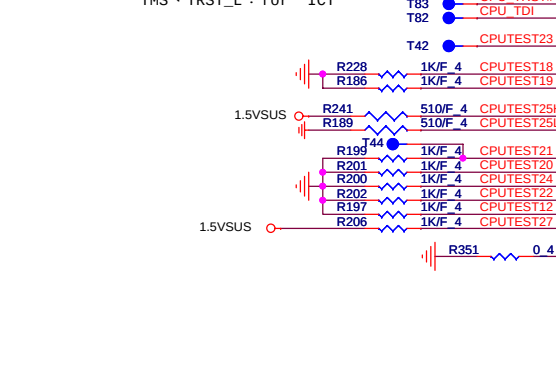




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2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as "Green Partners".



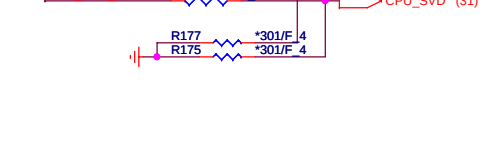
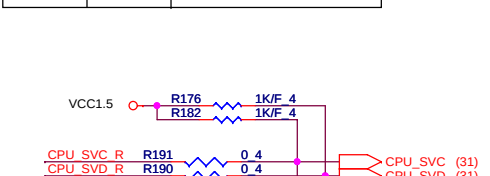
TDI - TD0 - TCK - TMS - TRST_L : for ICT



S1g4 does not support MEMHOT#



SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



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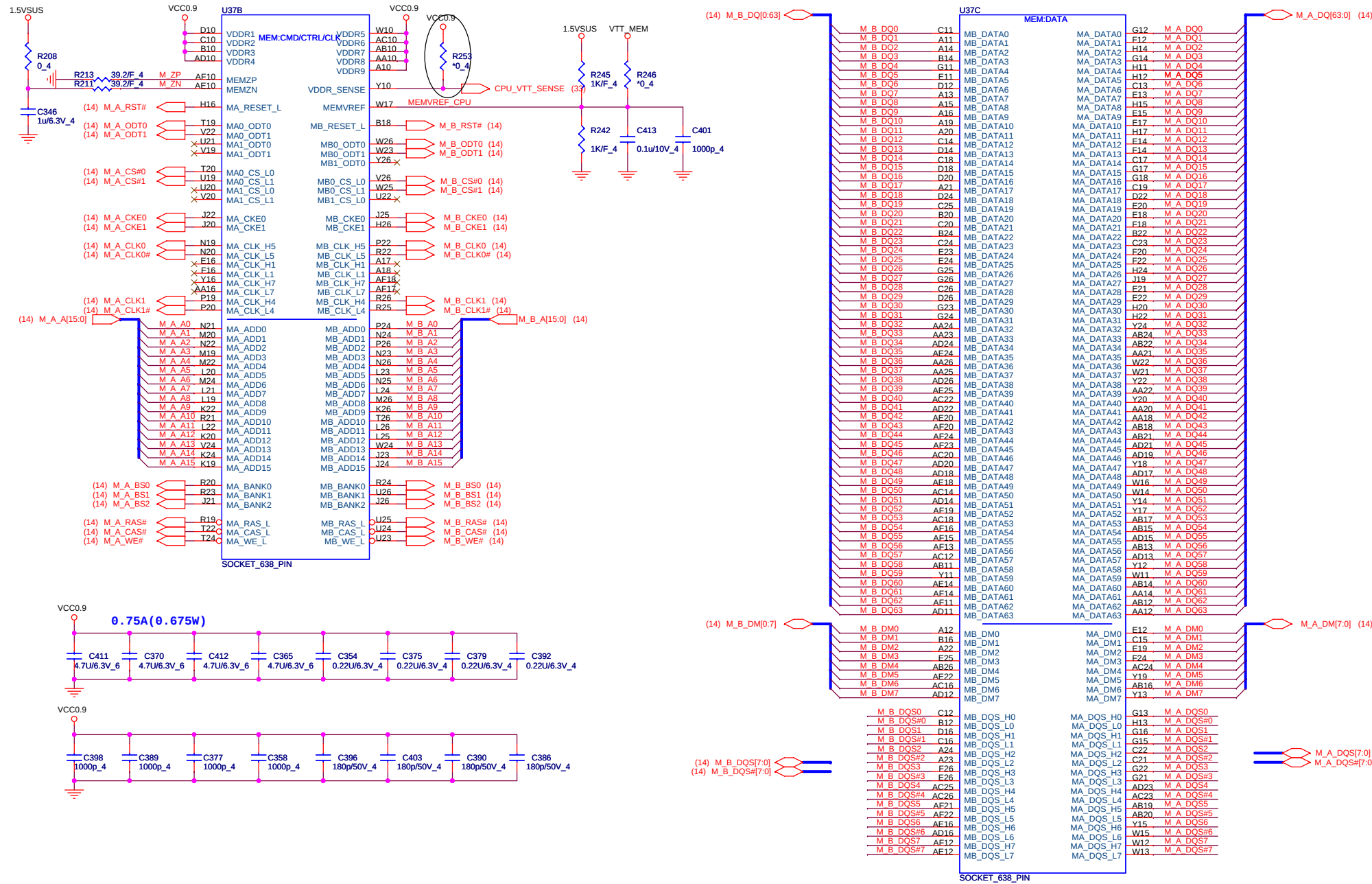
PROJECT : NE8

Size Document Number CPU HT/CONTROL(1/3) Rev 2A

Date: Wednesday, January 27, 2010 Sheet 3 of 42

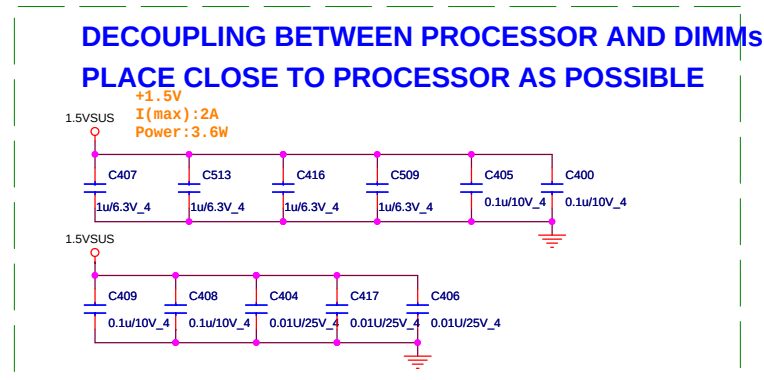
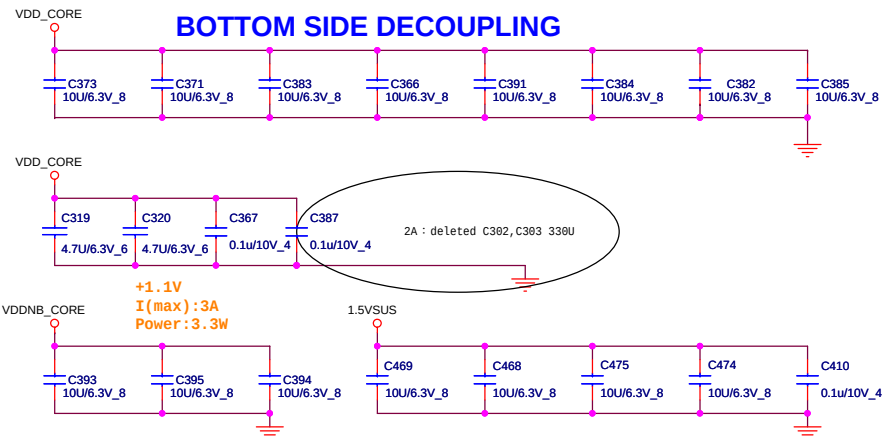
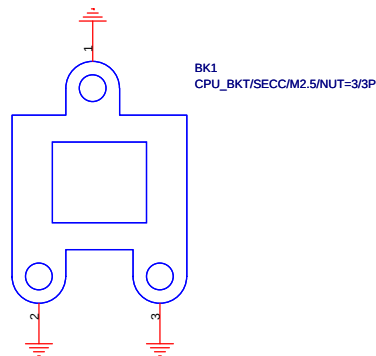
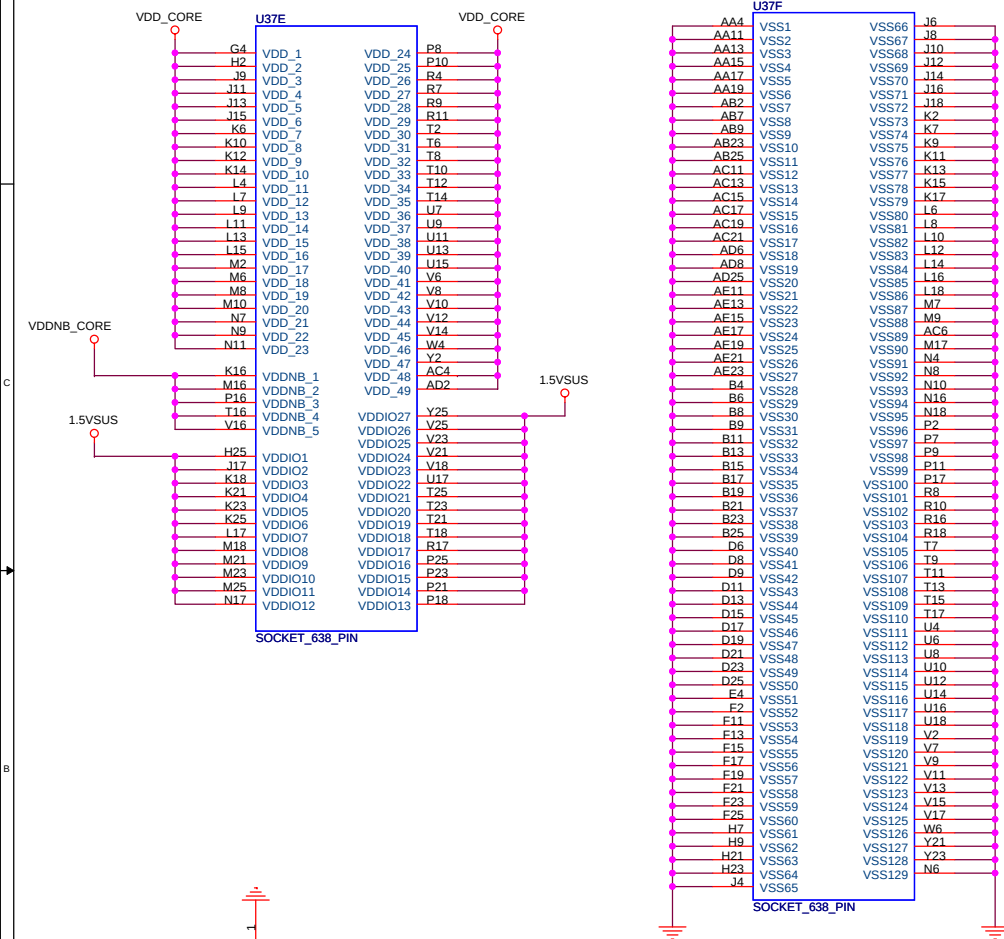
Processor Memory Interface

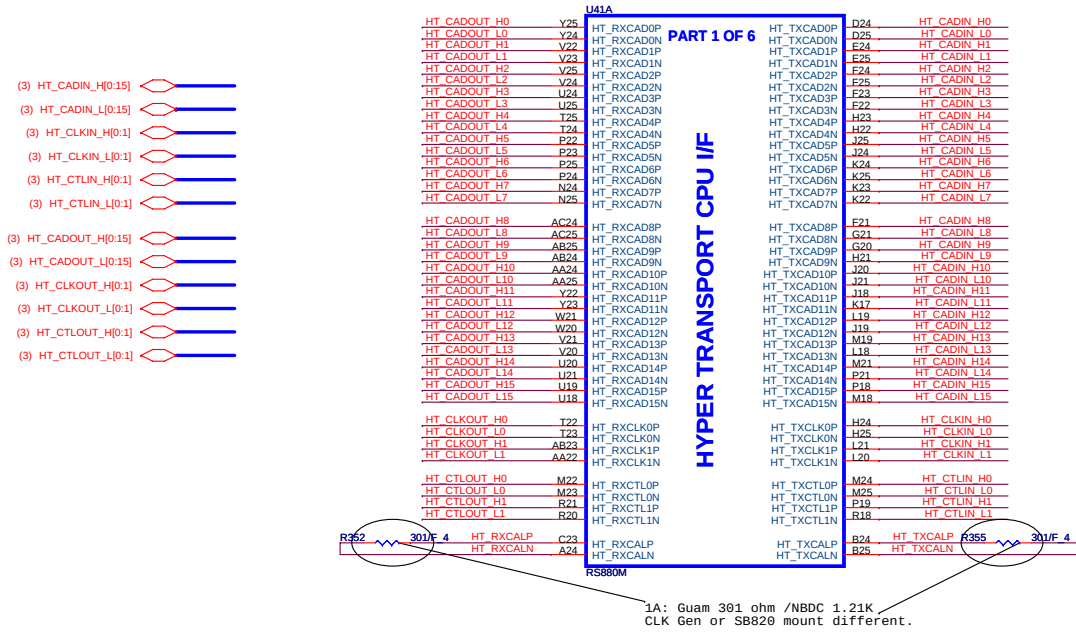
CPU_VDDR : 35W->0.9V
45W->1.05V



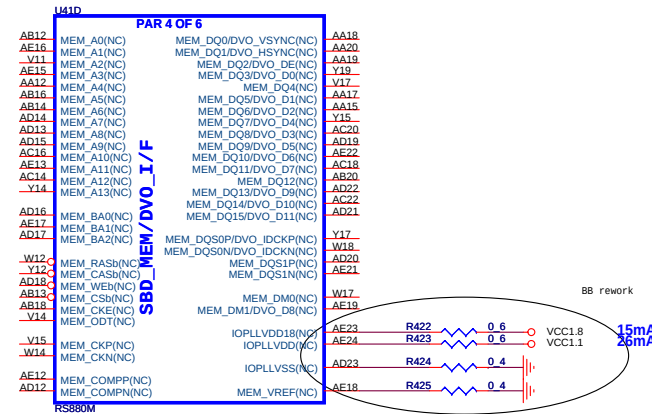
1.Level 1 Environment-related Substances should NEVER be Used.
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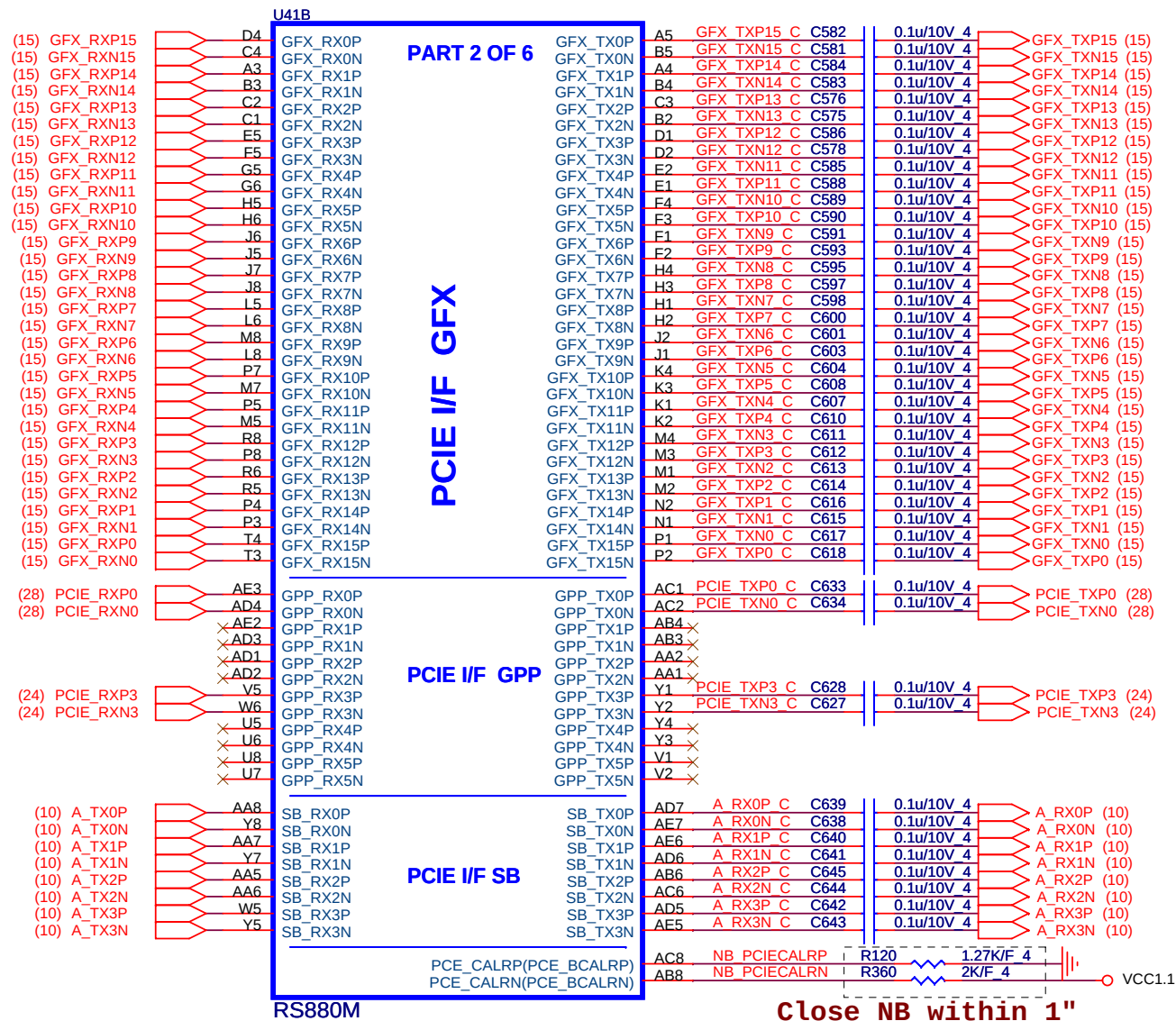
Socket Type	QCI P/N
Normal	DG0^8000018
90 degree	DG0^8000023





This block is for Side Port only , others can remove some components





Layout Swap
 TX11, TX10, TX9,
 TX8, TX7, TX6, TX5,
 TX4, TX3, TX2, TX0

GLAN

WLAN

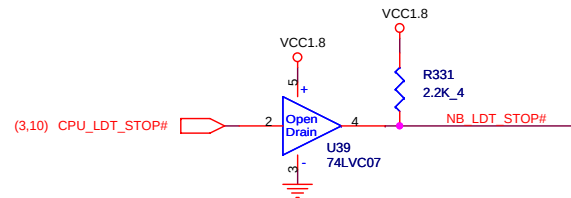
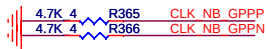
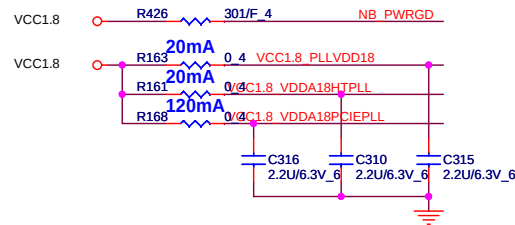
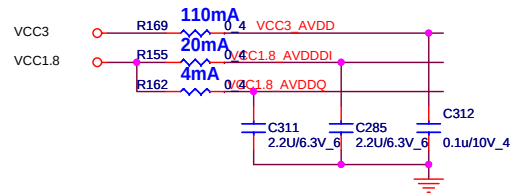


Quanta Computer Inc.

PROJECT : NE8

Size	Document Number	Rev
	RS880M GFX/PCIE(2/4)	2A
Date:	Wednesday, January 27, 2010	Sheet 7 of 42

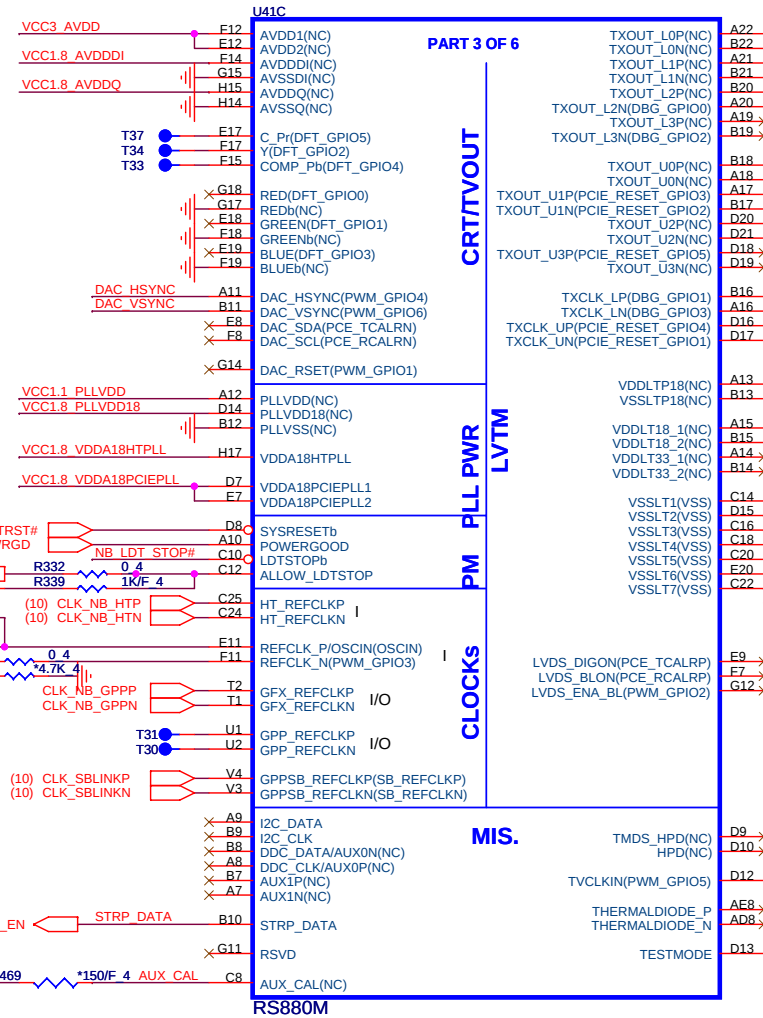
1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Enables Debug Bus access through memory I/O pads and GPIO.
0 : Enable RS880M, Default
1 : Disable RS880M

Discrete : Connect
A11, B11

Indicates if memory Side port is available or not
1: Disable side port memory
0: Enable side port memory



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Quanta Computer Inc. PROJECT : NE8		Rev 2A
Size	Document Number	
RS880M SYSTEM(3/4)		
Date:	Wednesday, January 27, 2010	Sheet 8 of 42



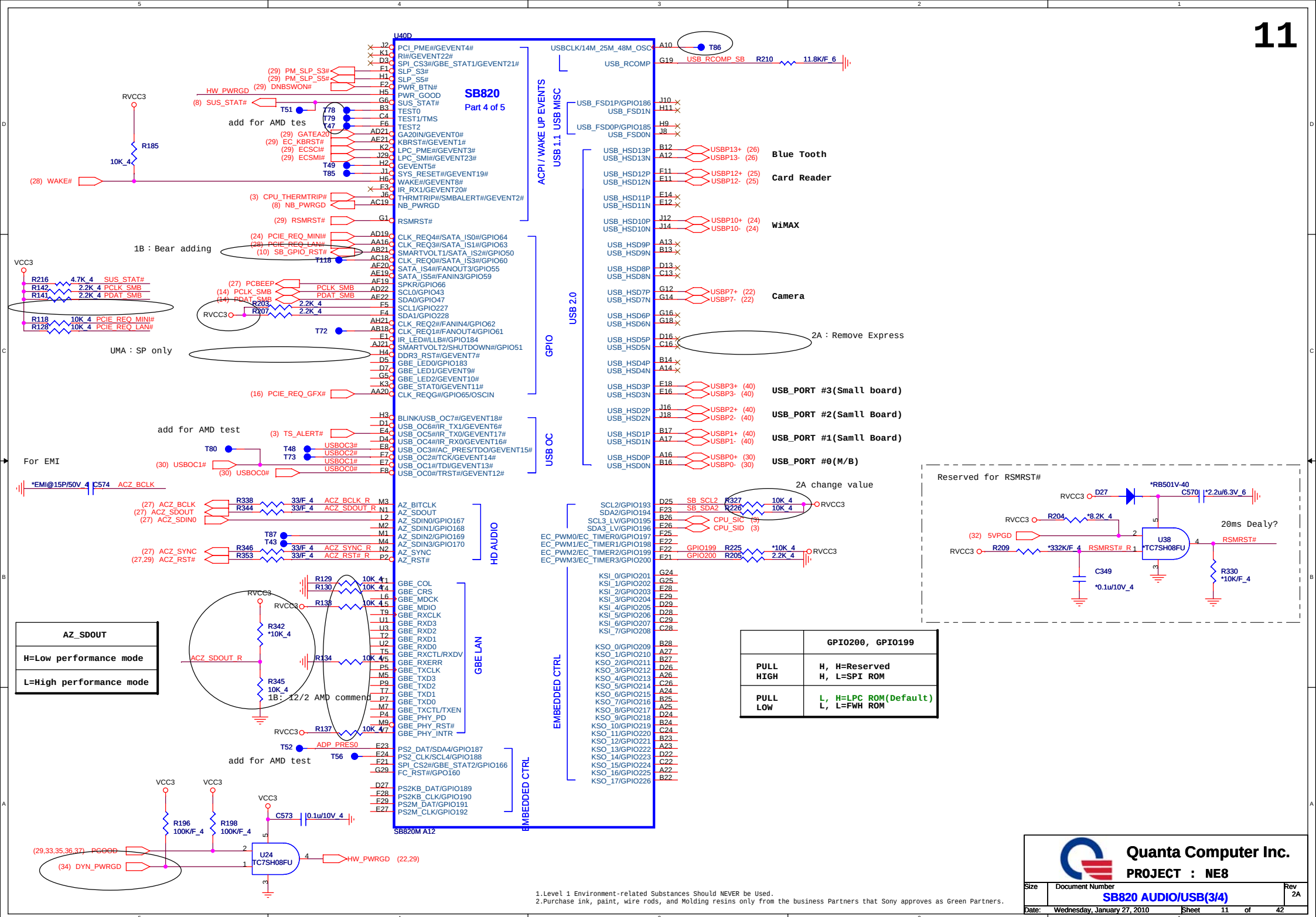
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D

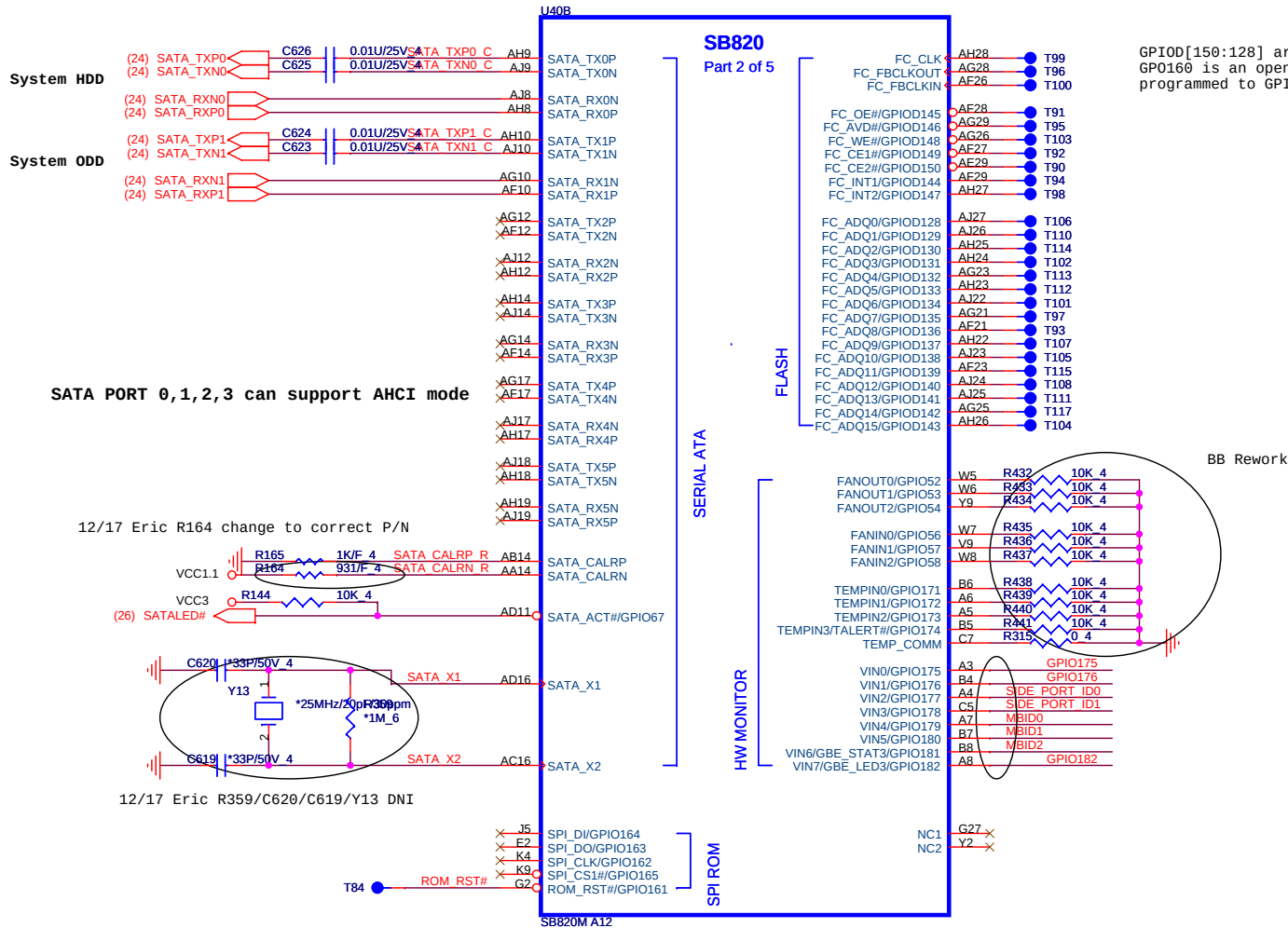
3

3

3



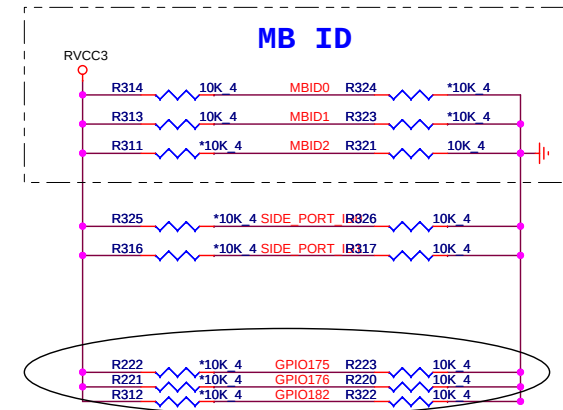
1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



GPIO[150:128] are open drain GPIO pins where as GP0160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

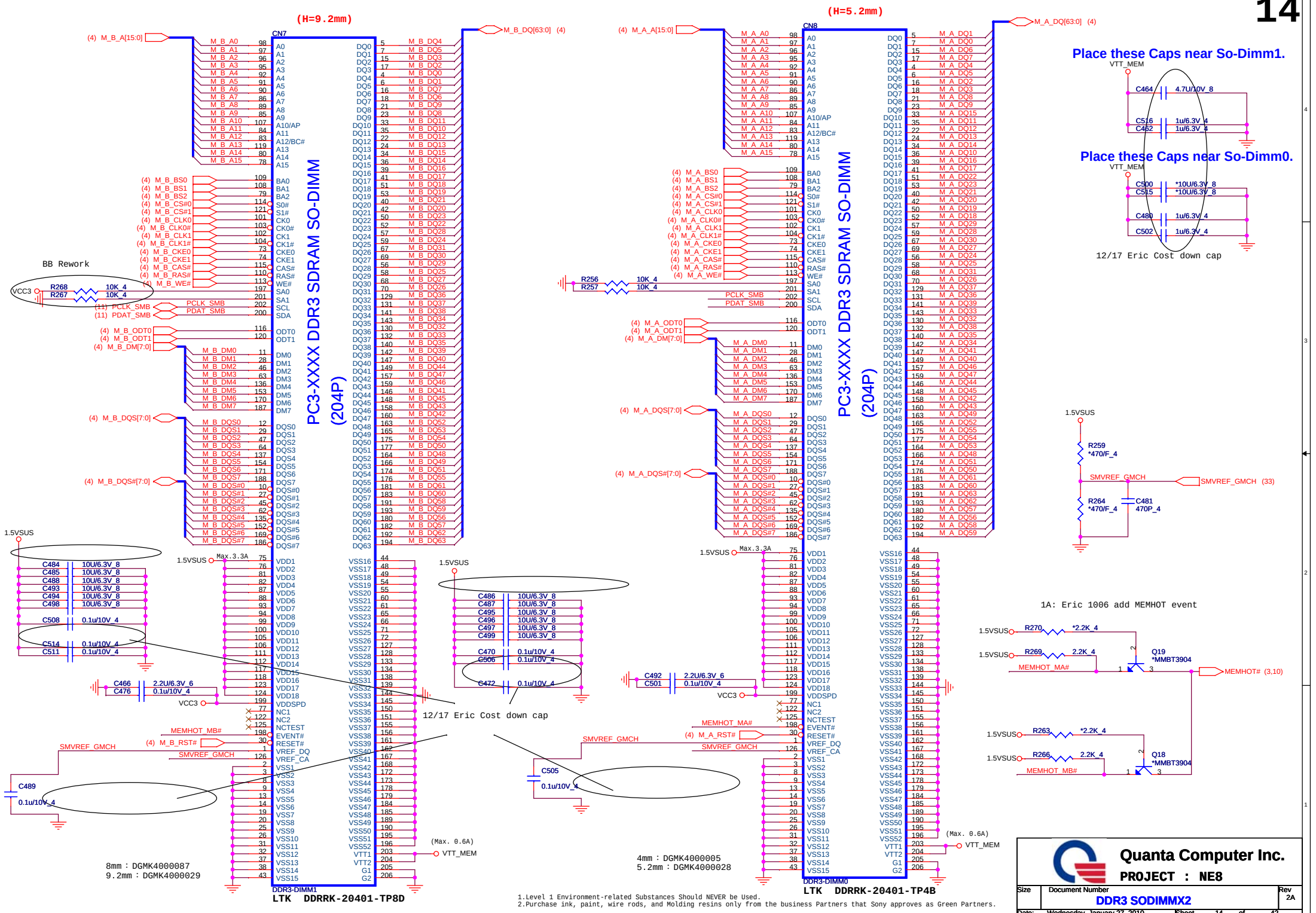
ID2	ID1	ID0	
0	0	0	Danube UMA
0	0	1	Danube UMA+Side port
0	1	0	Danube+Park XT
0	1	1	Danube+Madison LP
1	0	0	Danube+M92 XTX
1	0	1	
1	1	0	
1	1	1	

	NON	SAMSUNG	HYNIX	
SP ID0	0	1	0	1
SP ID1	0	0	1	1



- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





Place these Caps near So-Dimm1.0

Place these Caps near So-Dimm0.

12/17 Eric Cost down cap

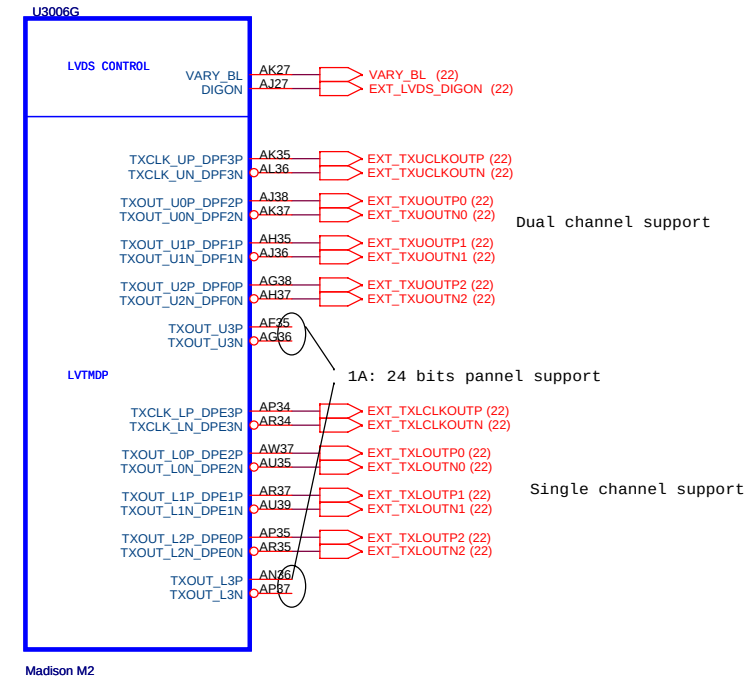
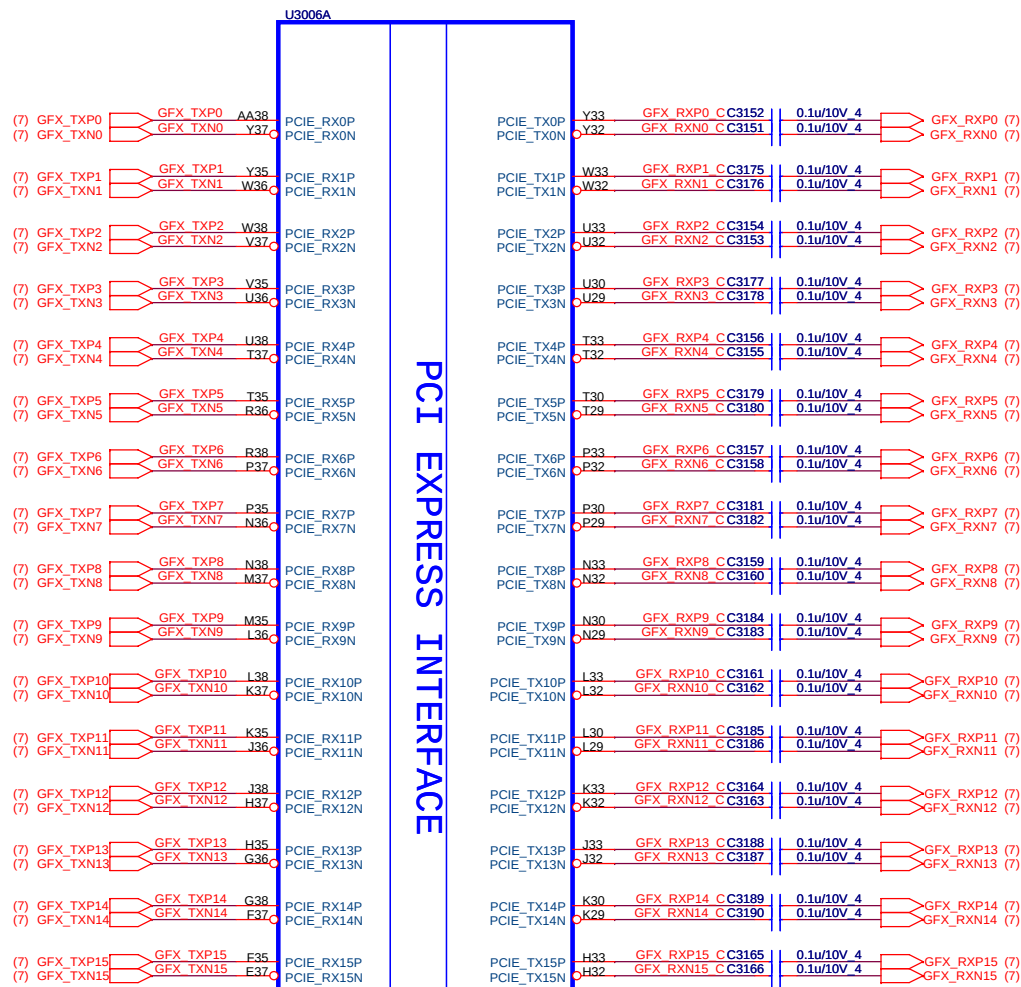
1A: Eric 1006 add MEMHOT event



Quanta Computer Inc.
PROJECT : NE8

Size	Document Number	Rev
	DDR3 SODIMMX2	2A
Date:	Wednesday, January 27, 2010	Sheet 14 of 42

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Madison M2

M9x : R3039 -> NC

Madison M2

1.Level 1 Environment-related Substances Should NEVER be Used.

2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Quanta Computer Inc.

PROJECT : NE8

Size	Document Number	Rev
	ATI PCIE/LVDS	2A
Date:	Wednesday, January 27, 2010	Sheet 15 of 42

AKD5LZGTW00
AKD5LGGT502
AKD5LGGT701

The diagram shows the T3000 pinout with the following connections:

- T3009 is connected to GFx GPIO0 (blue dot).
- T3002 is connected to GFx GPIO1 (blue dot).
- T3008 is connected to GFx GPIO2 (blue dot).
- T3001 is connected to GFx GPIO3 (blue dot).

Other signals shown include:

- (22) EXT_LVDS_BLON (red arrow pointing to a pin)
- GPIO9 (red line)
- GPIO11 (red line)
- GPIO12 (red line)
- GPIO13 (red line)
- (36) V_I2MPCNT0 (red arrow pointing to a pin)

(11) PCIE_REQ_GFX#

Deleted T3003 for layout (via is TP)

T3000

T3011

T3007

GPIO24 TRSTB

GPIO25 TDI

GPIO26 TCK

GPIO27 TMS

GPIO30 TDO

(23) EXT_HDMI_HPD ☐

The diagram shows the internal circuit of the Y3029 27MHz VCO. It features a central VCO component with two input/output pins, XTALIN and XTALOUT, which are connected to 22pF capacitors (C3230 and C3229). A feedback network is connected to the VCO, consisting of a 1u6F 3V_4 capacitor (C3199) and a 0.1u10V_4 capacitor (C3198) connected to the VCC1.8 and TSVD1 pins. The output of the VCO is labeled T_DPLUS and T_DMINUS.

```

U300D6B
MUT1 GFX

DVPNCNTL_MVP_0
DVPNCNTL_MVP_1
DVPNCNTL_0
DVPNCNTL_1
DVPNCNTL_2
DVPCLCK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23

```

I2C

GENERAL PURPOSE I/O

GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HP2D
GPIO_15_PWRCNTL_0
GPIO_16_SSEN
GPIO_17_THERMAL_IN
GPIO_18_HP2D3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERIC8
GENERICB
GENERICC
GENERICD
GENERICF_HP2D4
GENERICF

HPD1

VREFG

DPLL_PVDD

DPLL_PVSS

PLL/CLOCK

XTALIN
XTALOUT
XO_IN
XO_IN2

DPLUS
DMINUS

TS_FDO
TS_A

TSVDD
TSVSS

THERMAL

PA	TXC4P_DPA3P TXC4M_DPA3N	AU24 AV23	EXT_HDMI_TXCN0 (2) EXT_HDMI_TXCN1 (2)
PB	TX0P_DPA2P TX0M_DPA2N	AT25 AR24	EXT_HDMI_TX0P0 EXT_HDMI_TX0N0
	TX1P_DPA1P TX1M_DPA1N	AU26 AV25	EXT_HDMI_TX0P1 EXT_HDMI_TX0N1
	TX2P_DPA0P TX2M_DPA0N	AT27 AR26	EXT_HDMI_TX0P2 EXT_HDMI_TX0N2
	TXCBP_DPB3P TXCBM_DPB3N	AR39 AT28	
	TX3P_DPB2P TX3M_DPB2N	AV31 AU30	
	TX4P_DPB1P TX4M_DPB1N	AR32 AT31	
	TXSP_DPB0P TXSM_DPB0N	AT33 AU33	
	TXCCP_DPC3P TXCCM_DPC3N	AU34 AV33	
	TX0P_DPC2P TX0M_DPC2N	AT15 AR14	
	TX1P_DPC1P TX1M_DPC1N	AU15 AV15	
TX2P_DPC0P TX2M_DPC0N	AR16 AT16		
TXCDP_DPD3P TXCDM_DPD3N	AU29 AT18		
TX3P_DPD2P TX3M_DPD2N	AT21 AR20		
TX4P_DPD1P TX4M_DPD1N	AU22 AV22		
TXSP_DPD0P TXSM_DPD0N	AT23 AR23		

AD39
AD37

AC36

H2SYNC	AD29	X
V2SYNC	AC29	X

DC/AUX

Signal	Pin	Signal	Pin
DDC1CLK	AM26	EXT_HDMI_SCL	(23)
DDC1DATA	AN26	EXT_HDMI_SDA	(23)

DDC2CLK AM19
 DDC2DATA AL19
 AUX2P AN20
 AUX2N AM20
 DDCCLK_AUX3P AL30
 DDCDATA_AUX3N AM30

DDCDATA_AUX4N AM2X

DDCCLK_AUX5P AM21

DDCDATA_AUX5N AM2X

DDC6CLK A330 CRT_SCL (22)

DDC6DATA A331 CRT_SDA (22)

DDCCLK_AUX7P AK30

DDCDATA_AUX7N AK29

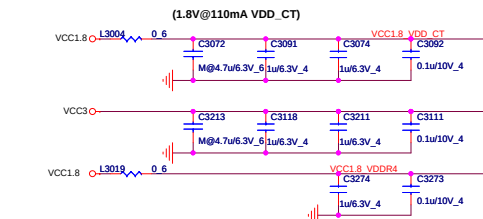
CRT_HSYNC (22)

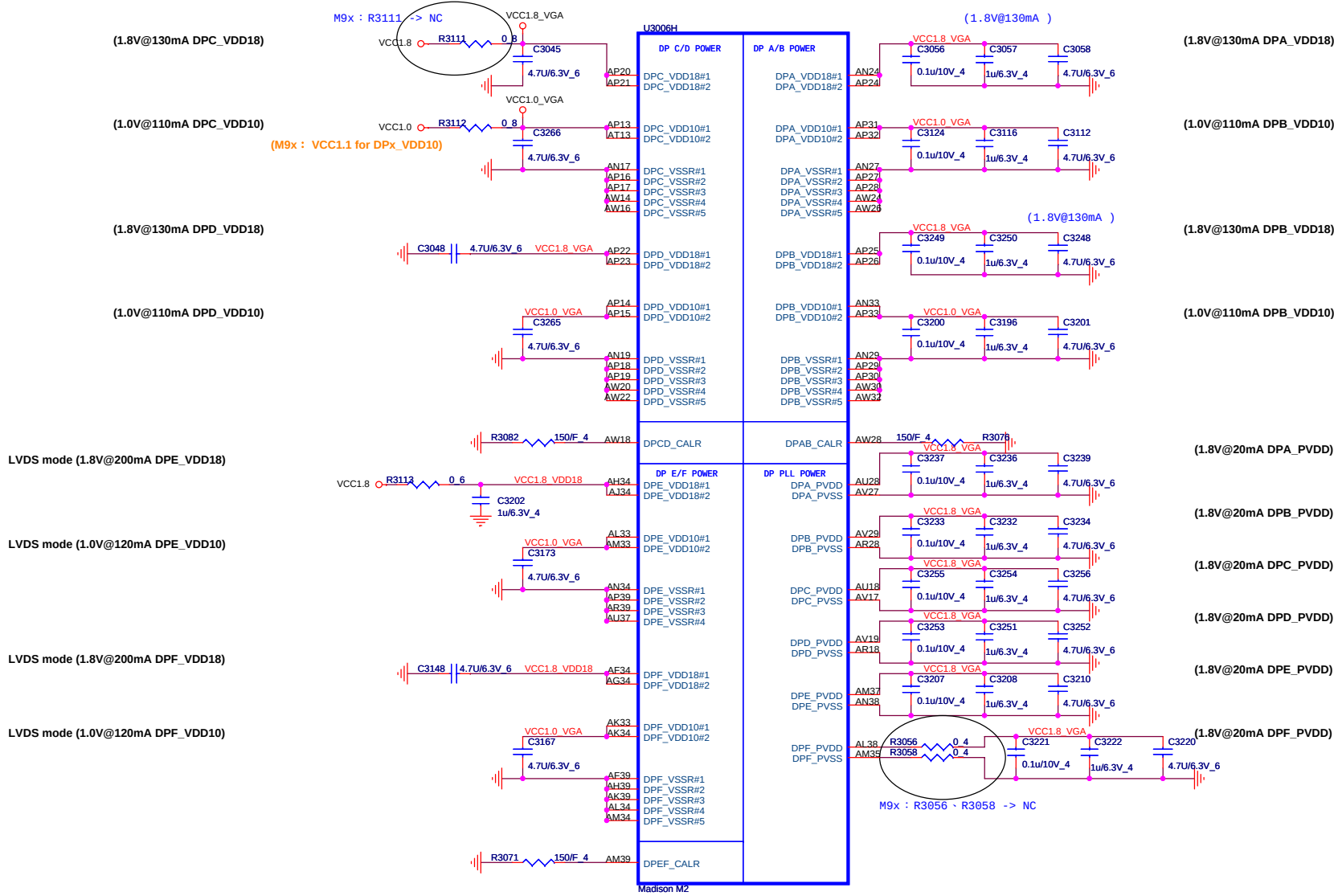
100



 **Quanta Computer Inc.**
PROJECT : NE8

(For Park&DDR3, VDDR = 1.5V@2.0A)

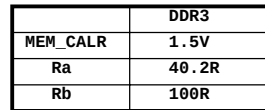




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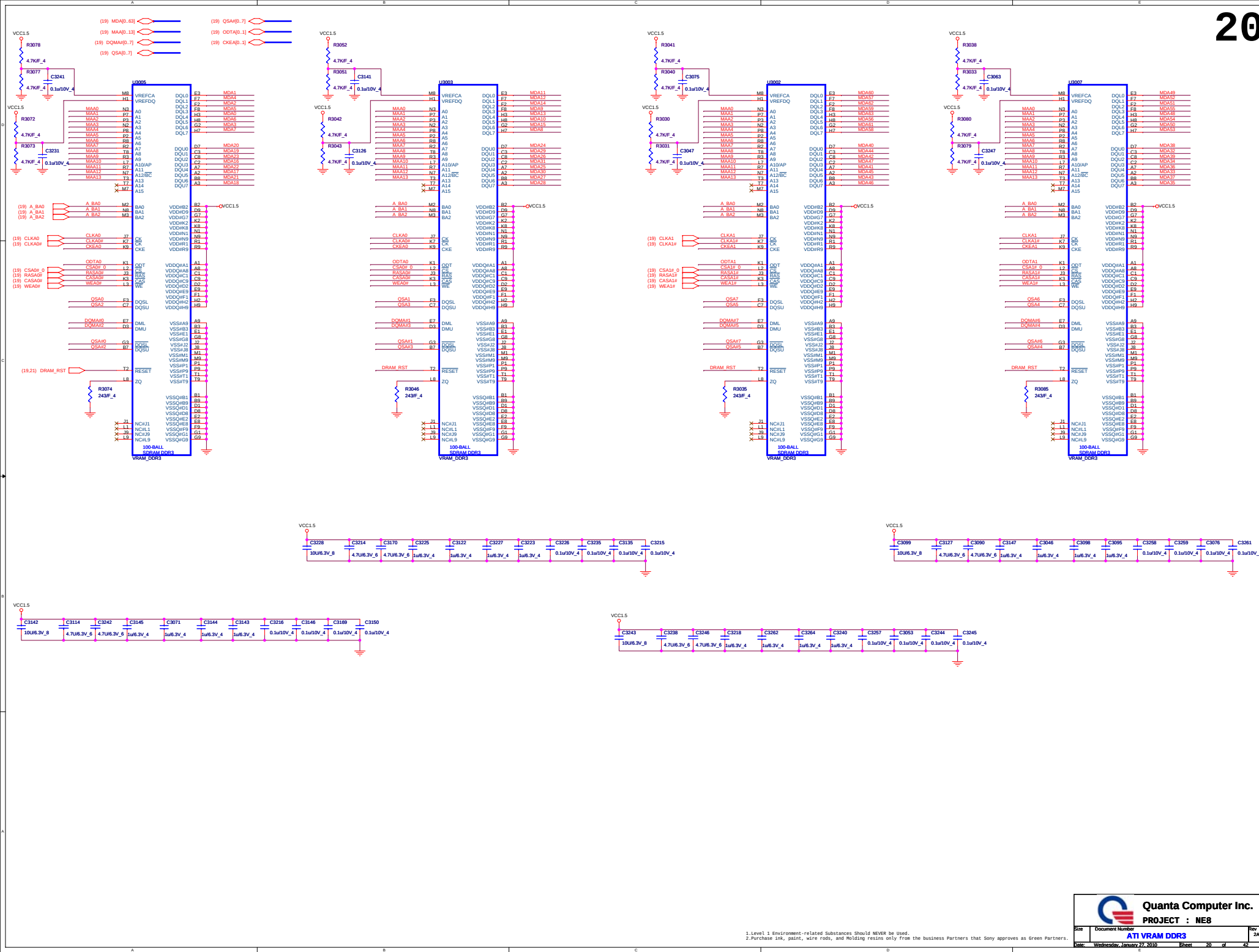
 Quanta Computer Inc. PROJECT : NE8		Size	Document Number	Rev	
		ATI MEM/IF/DP	2A		
Date:	Wednesday, January 27, 2010	Sheet	18	of	42

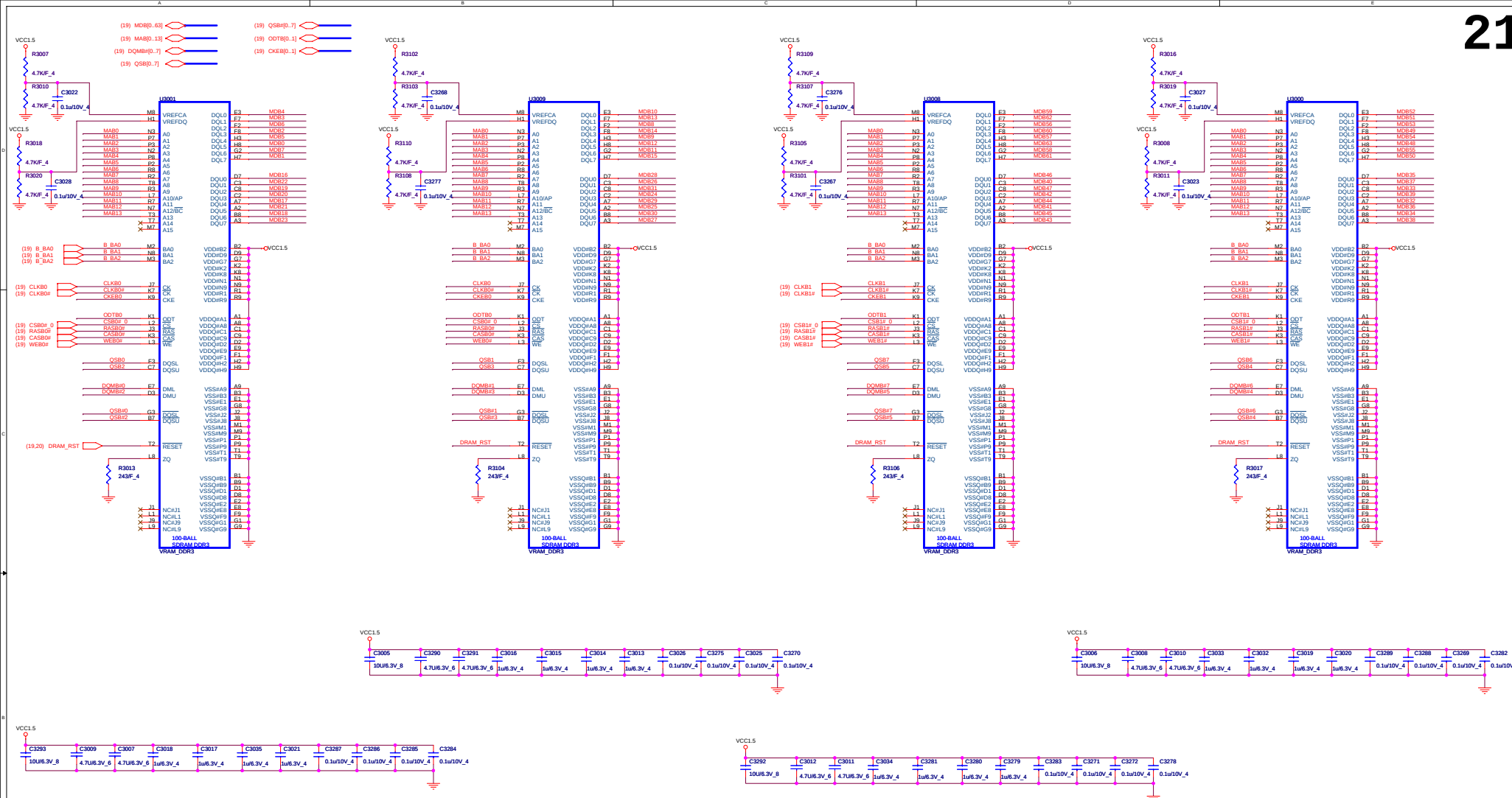
Use this option ONLY
for Park-S3



 Quanta Computer Inc. PROJECT : NE8		
Size	Document Number	Rev
	ATI MEM IF	2A
Date:	Wednesday, January 27, 2010	Sheet 19 of 42

**Use this option ONLY
for Park-S3**

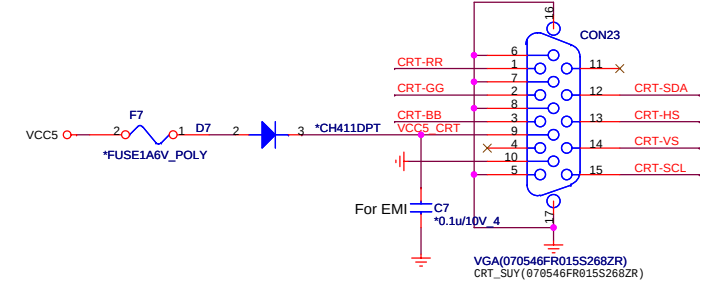
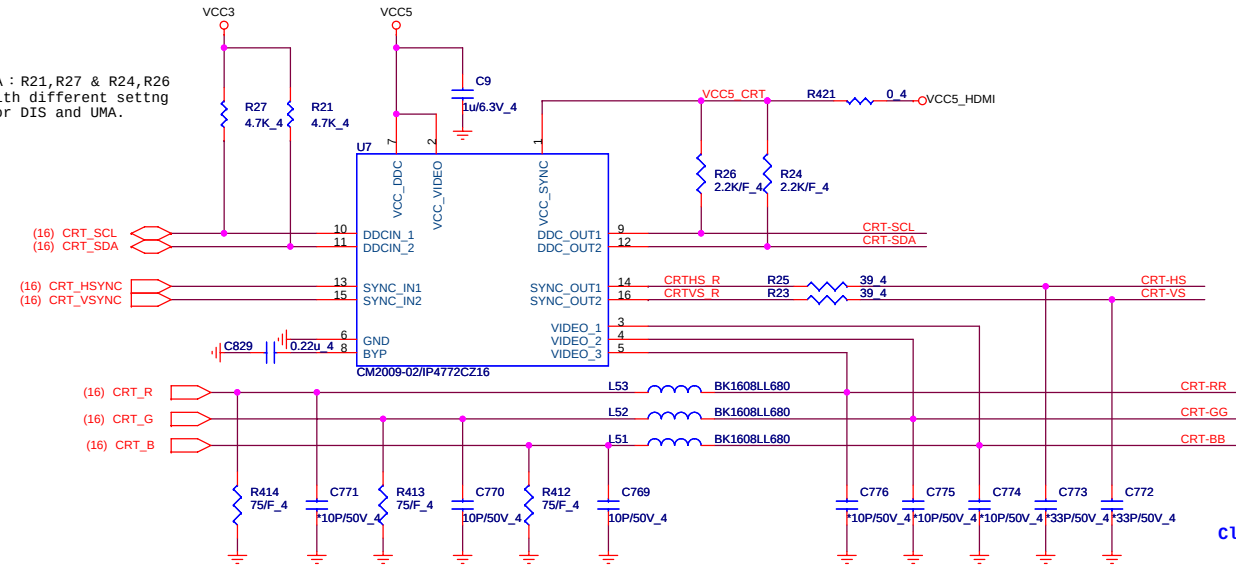




CRT

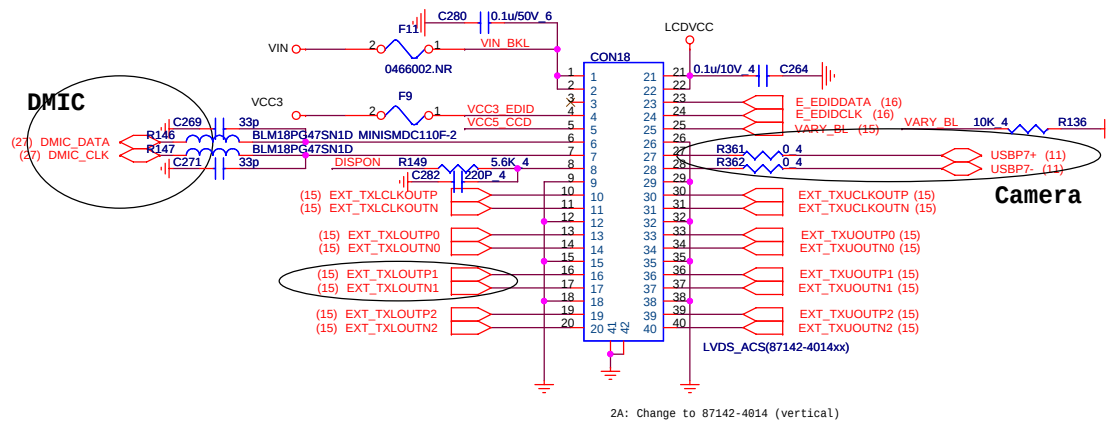
22

2A : R21,R27 & R24,R26
with different setting
for DIS and UMA.



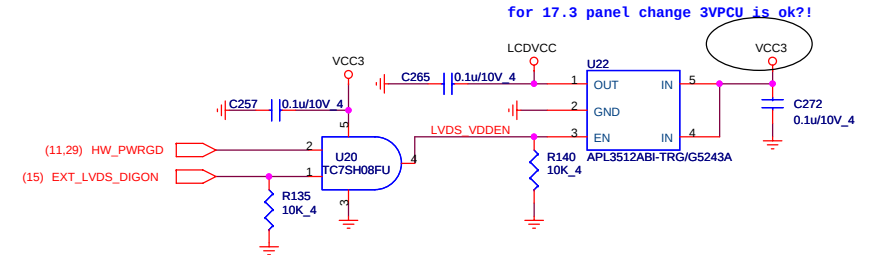
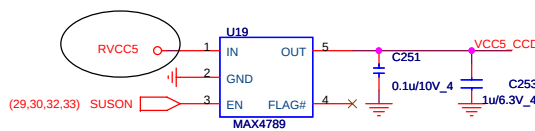
Close to Con3

LVDS

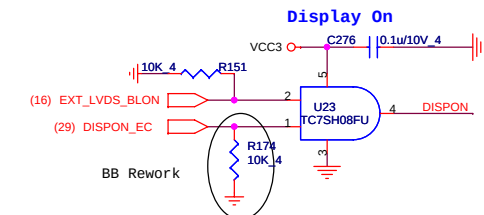


2A: Change to 87142-4014 (vertical)

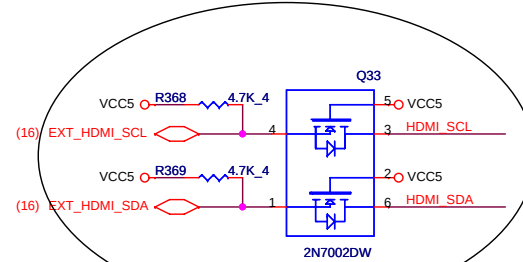
1C: 12/17 add RVCC5 for optional power source



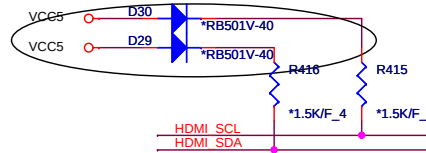
for 17.3 panel change 3VPCU is ok?!



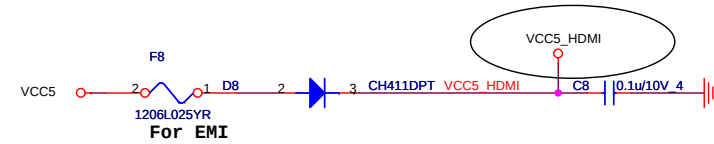
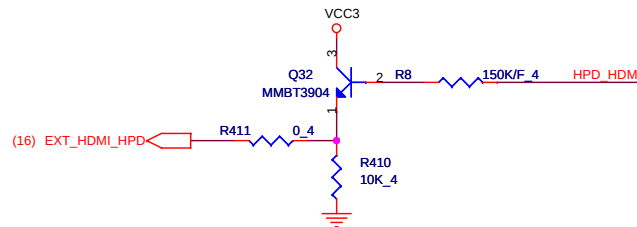
1B: share power with CRT port



1B: add diode for HDMI test



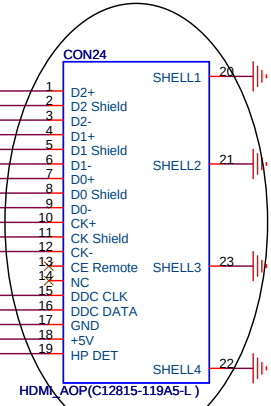
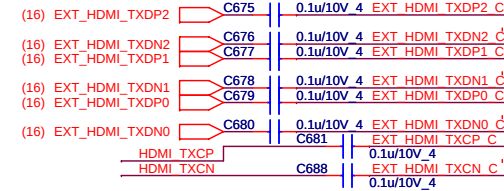
12/17 Eric D29/D30/R416/R415 DNI



For EMI



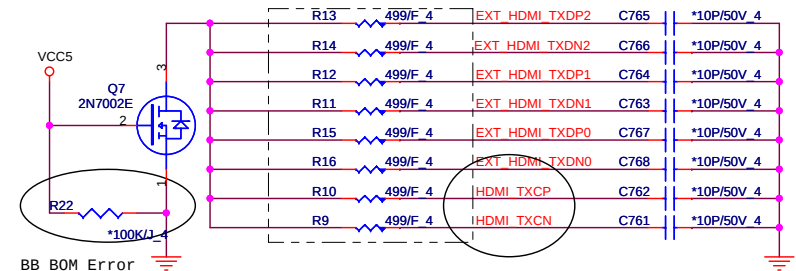
ATI Suggestion close to Con24



0115 change connector, need update P/N

ATI Suggestion close to Con24

For ESD



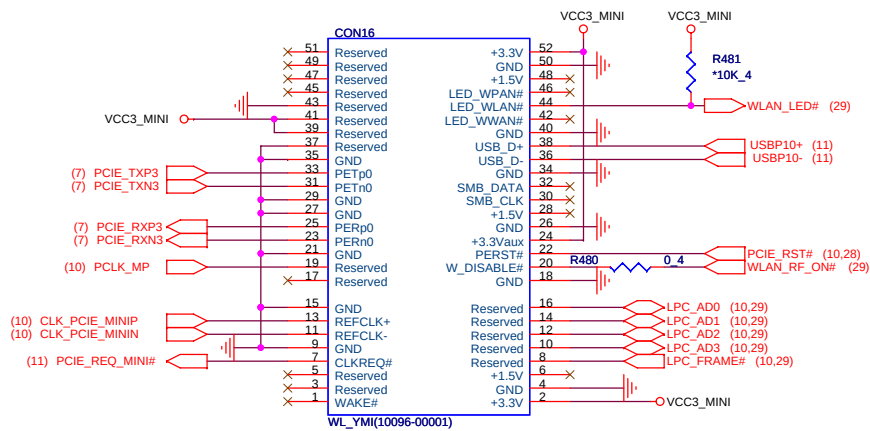
BB BOM Error
100K ohm
12/17 Eric R22 DNI

Quanta Computer Inc.

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	HDMI	2A
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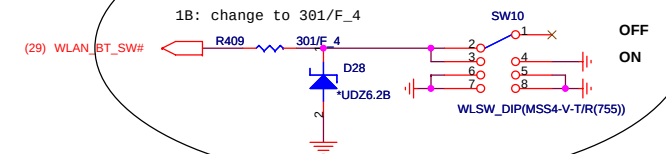
1.Level 1 Environment-related Substances Should NEVER be Used.
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Win7 didn't support wake WLAN

2A need check TOP or BOT again

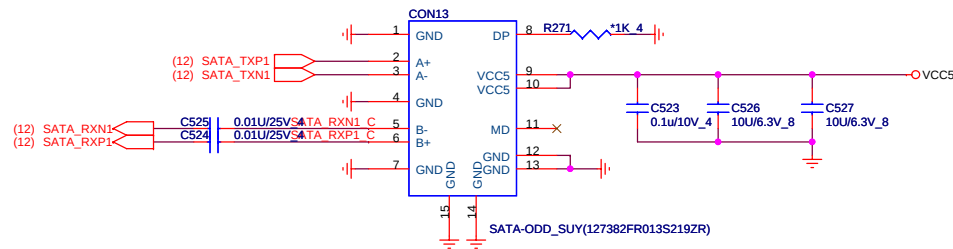
WLAN_BT_SW



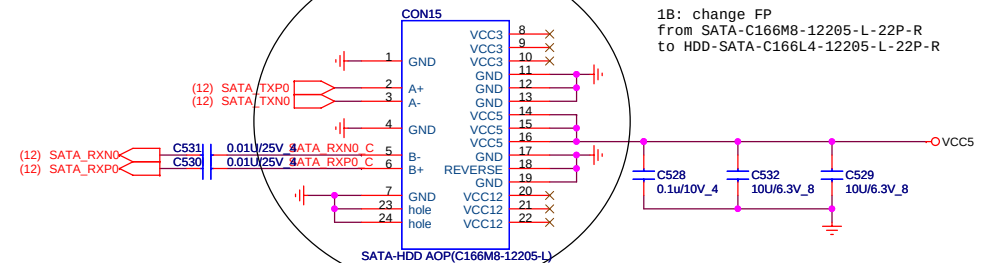
BTM Side , Right==>ON

2A : deleted VCC1.5_MINI

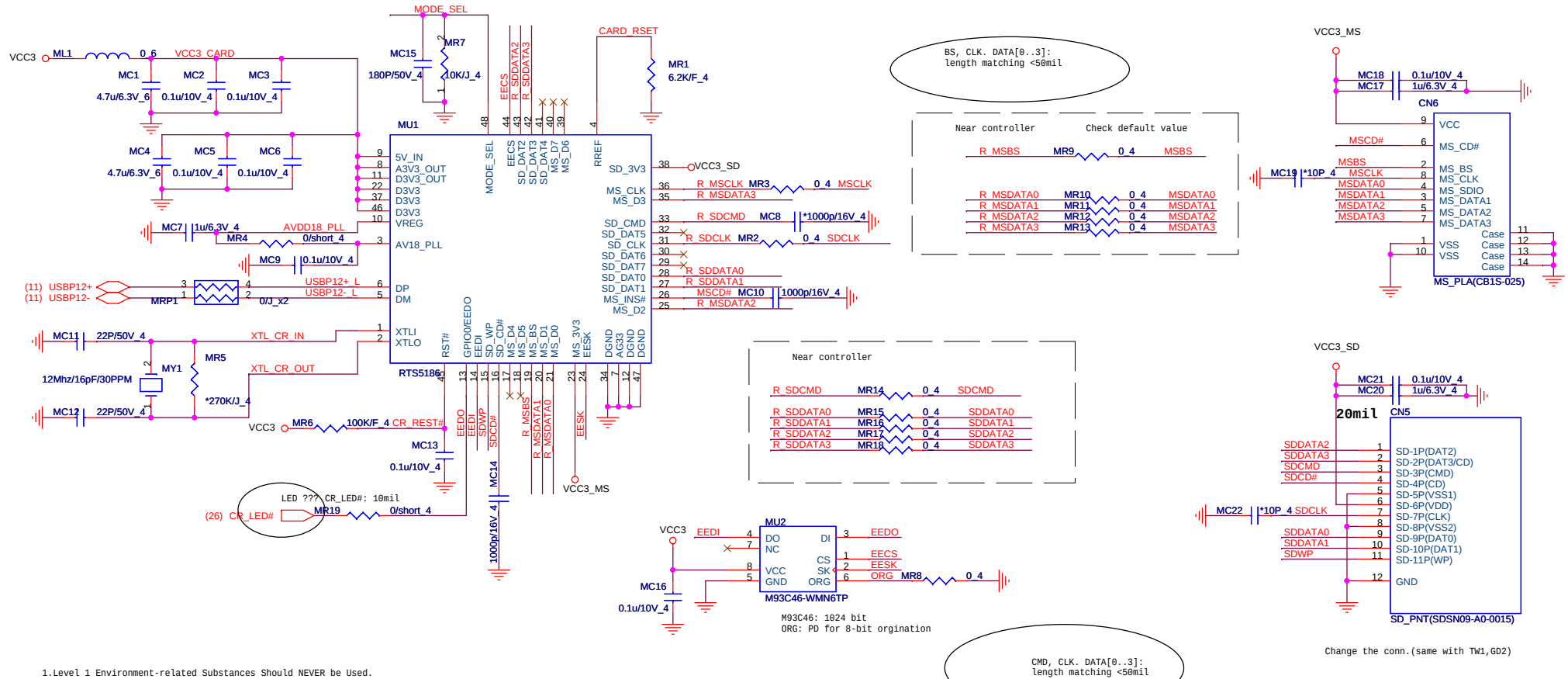
SATA ODD



2.5 inch SATA HDD



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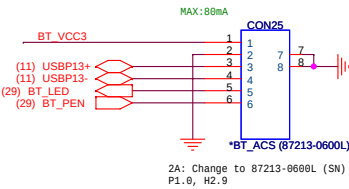
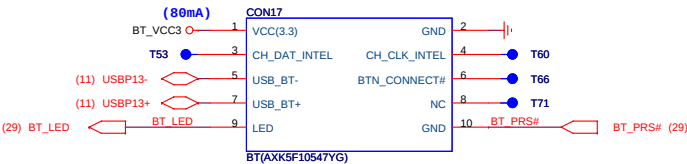
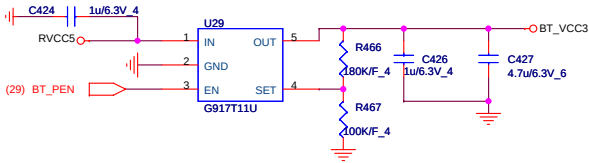


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	CARD Reader	2A
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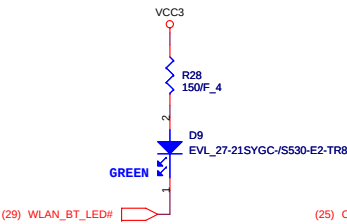
2A : Remove Express card

Bluetooth

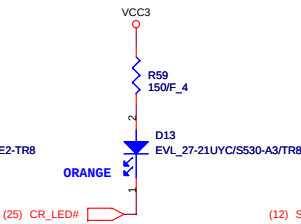


000M--BC2070 (wire)
1. 3.3V
2. GND
3. USB D+
4. USB D-
5. BT_LED
6. BT_ON

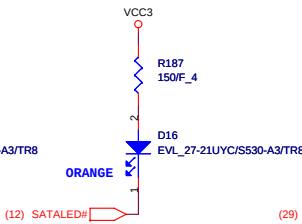
RF LED



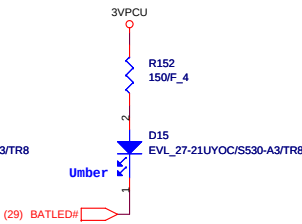
Card LED

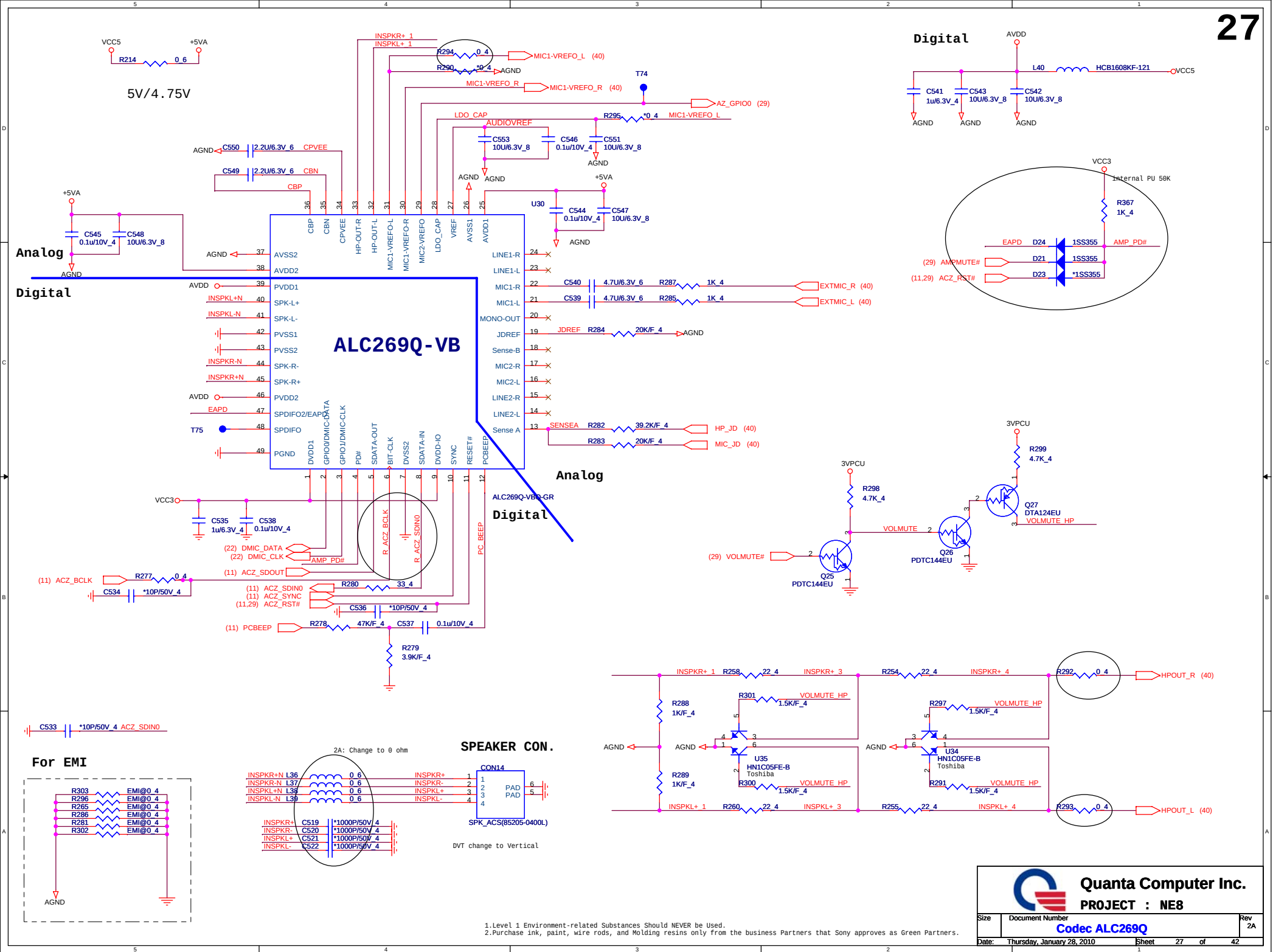


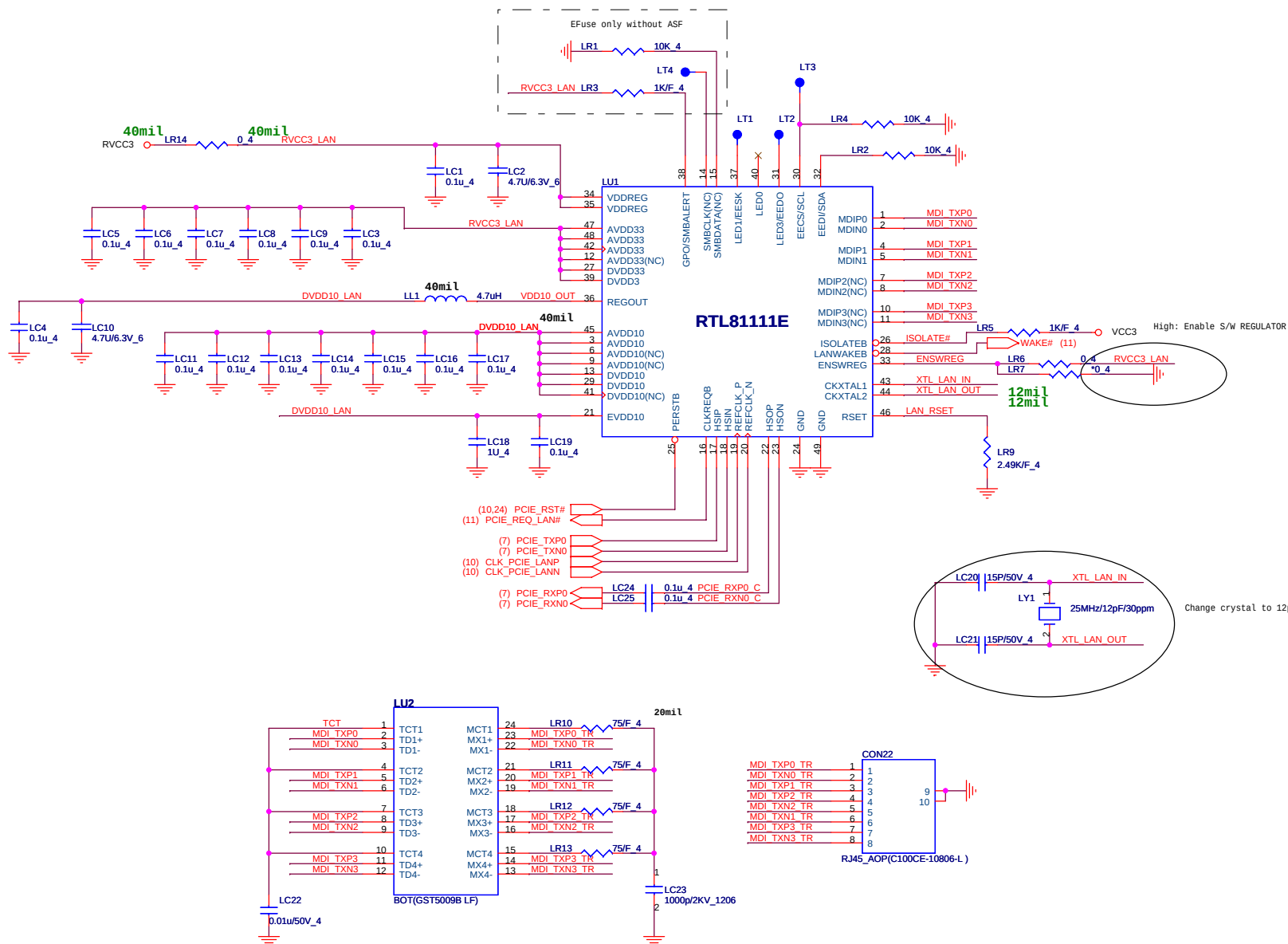
HDD LED



Battery LED

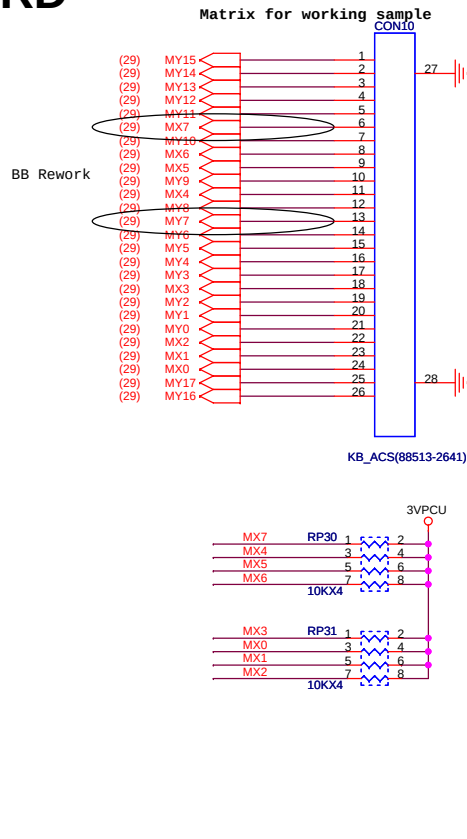




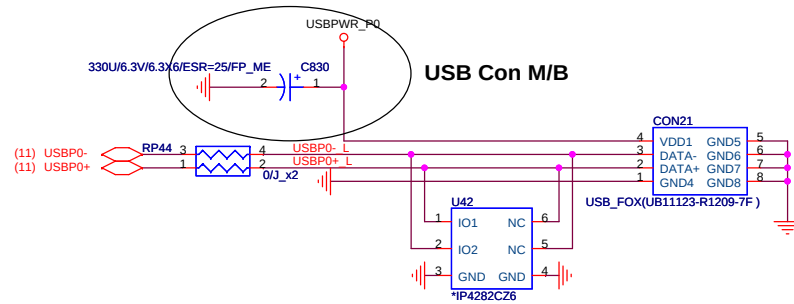
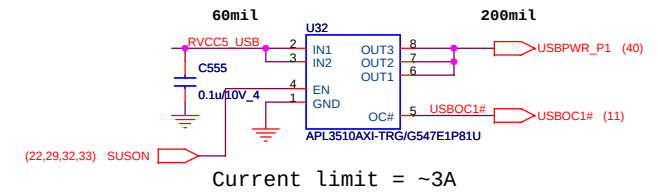
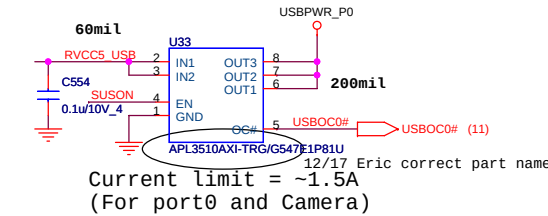


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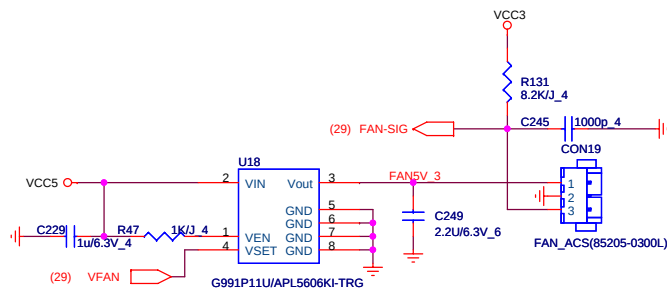
KEYBOARD



USB Port + e-SATA(USB)

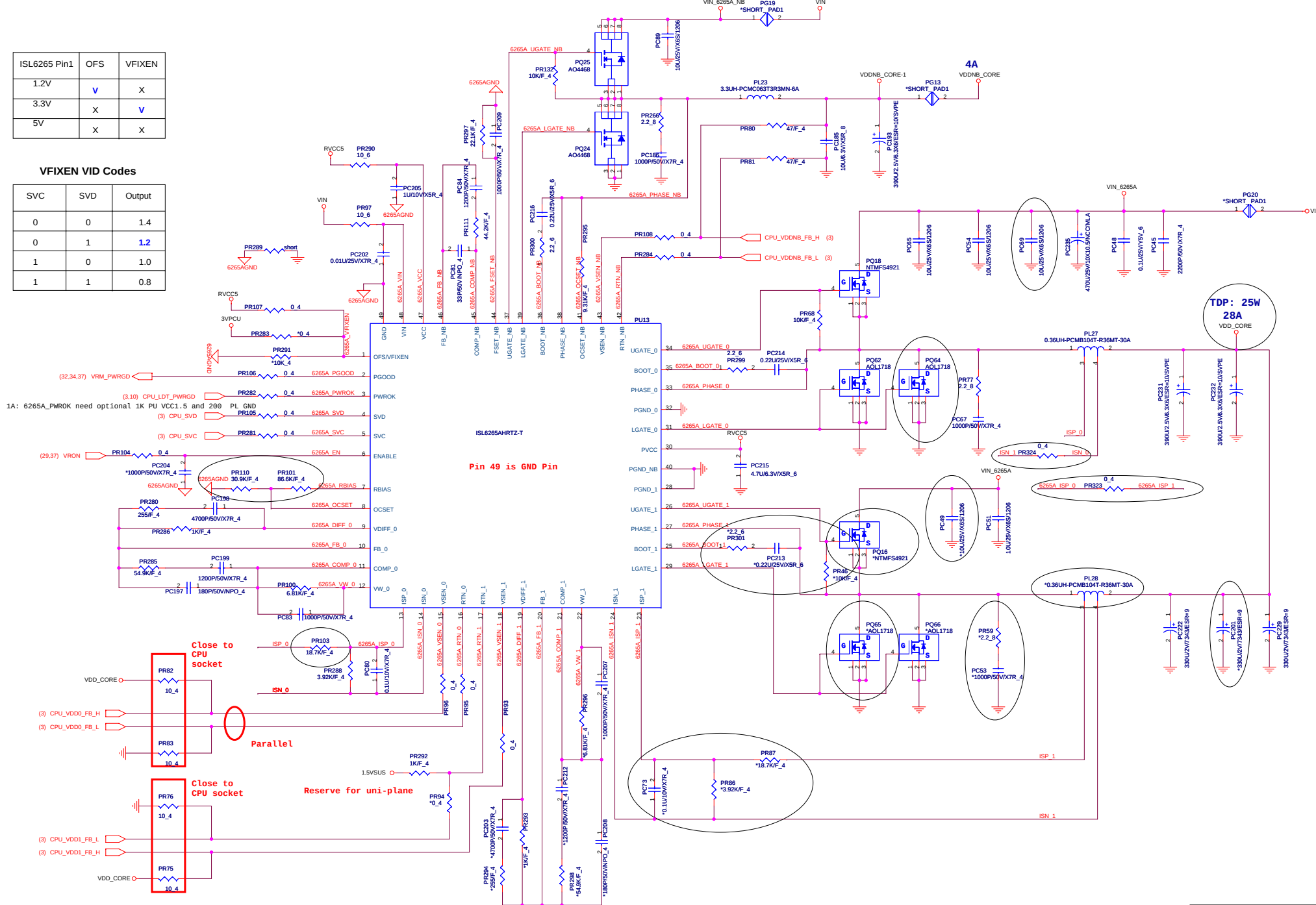


FAN

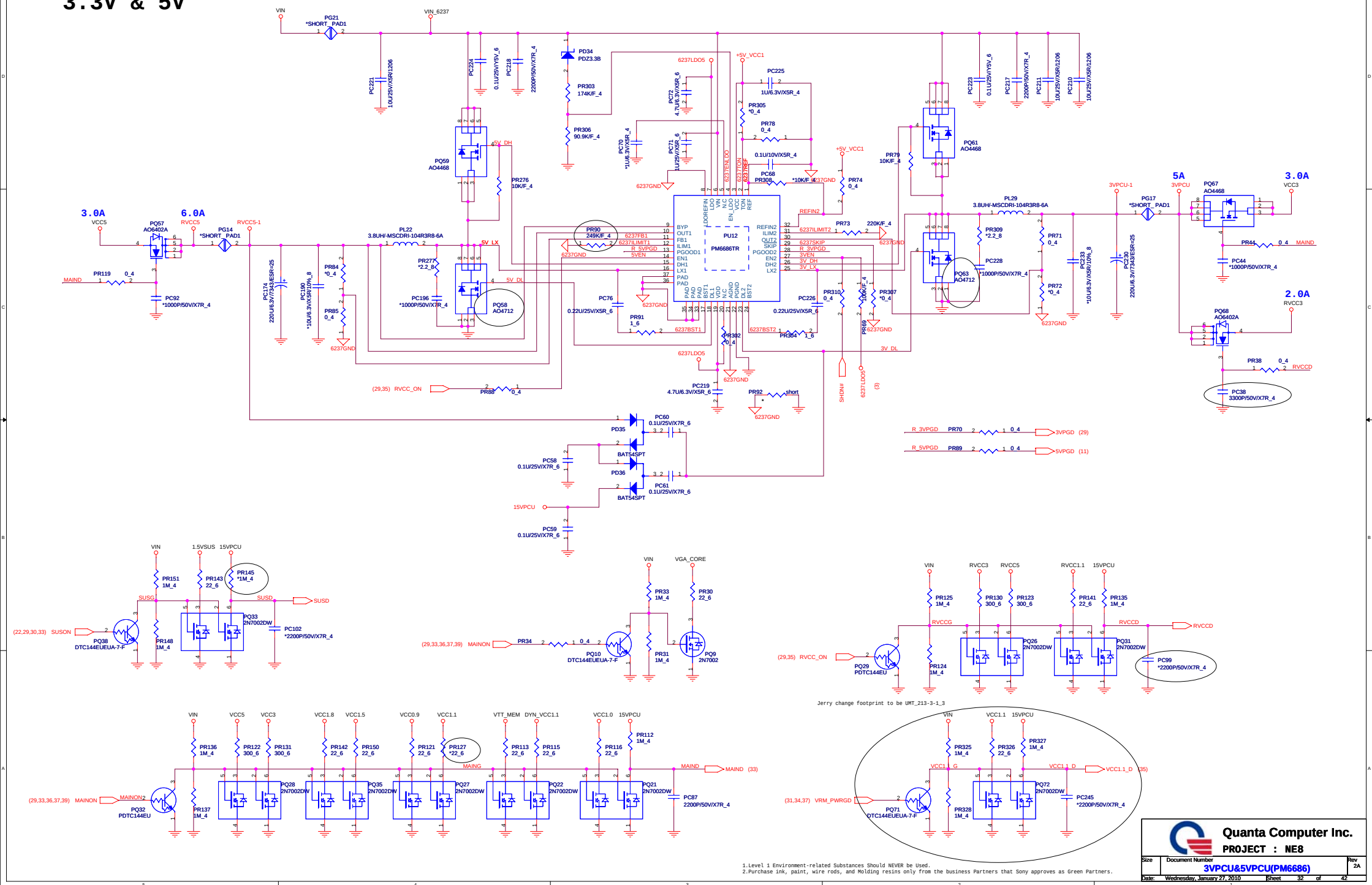


VFIXEN VID Codes

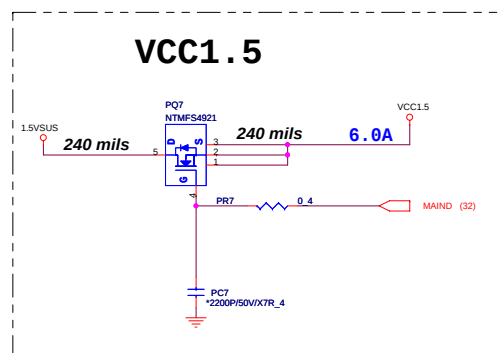
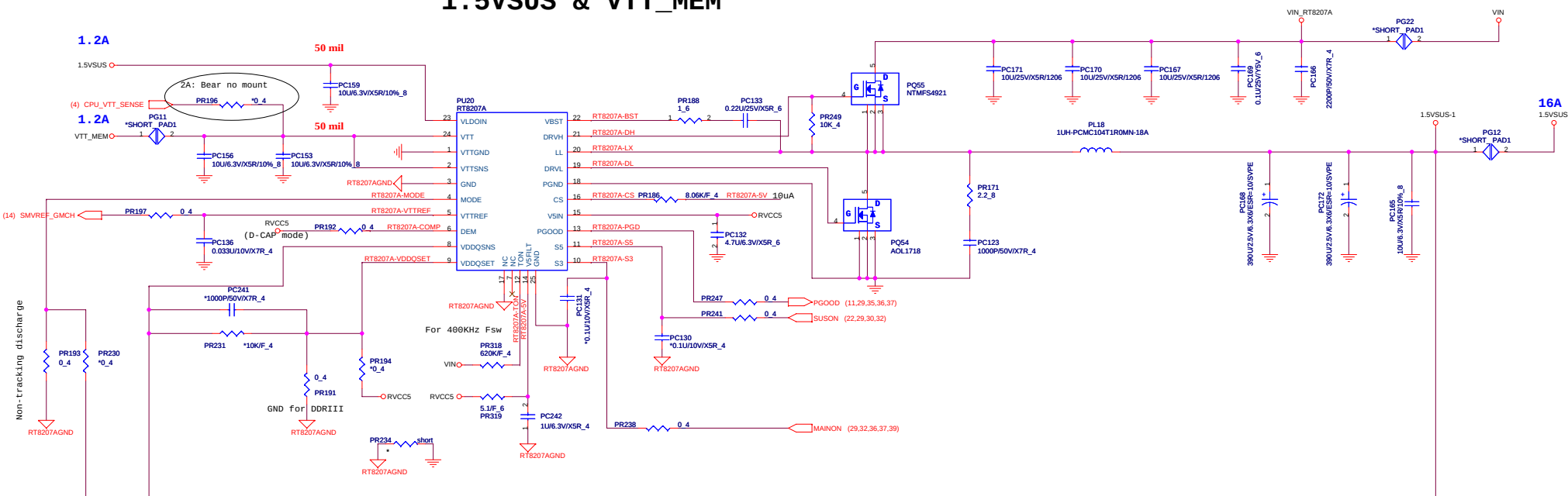
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



3.3V & 5V



1.5VSUS & VTT_MEM

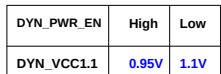


MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

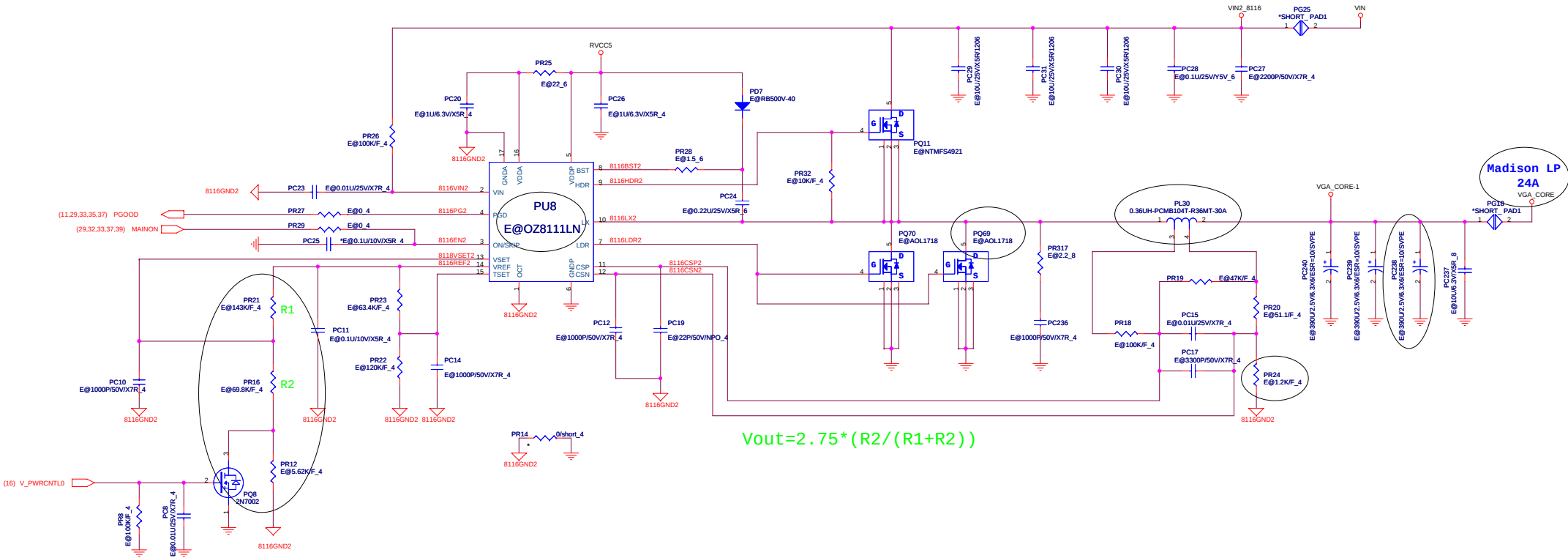
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.75V$$

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off







$$V_{out} = 2.75 * (R2 / (R1 + R2))$$

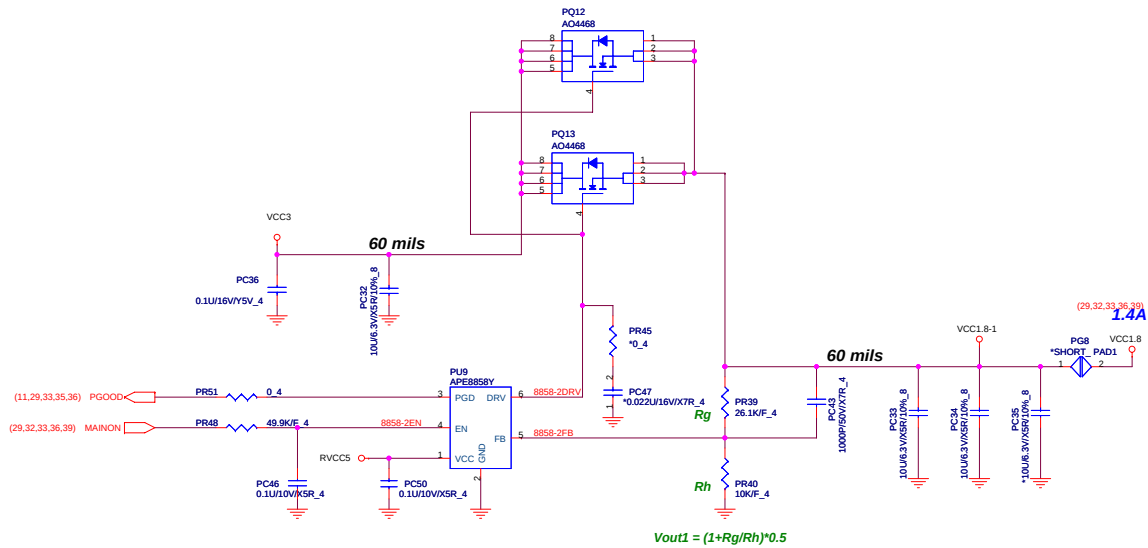
Madison LP

External VGA_CORE Voltage Setting:

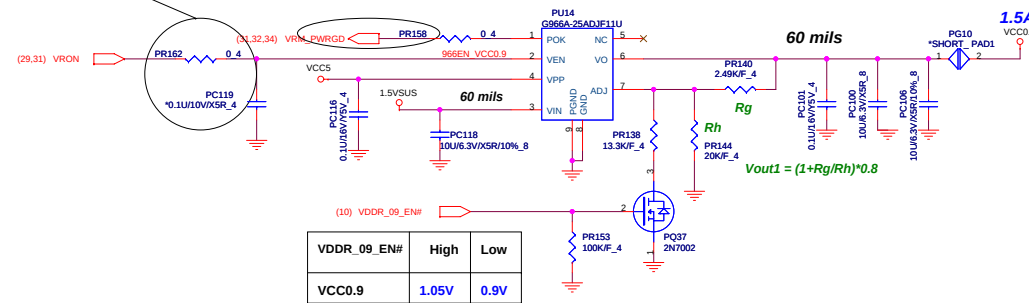
V_PWRCNTL0	VGA_CORE
0	0.95V
1	0.90V

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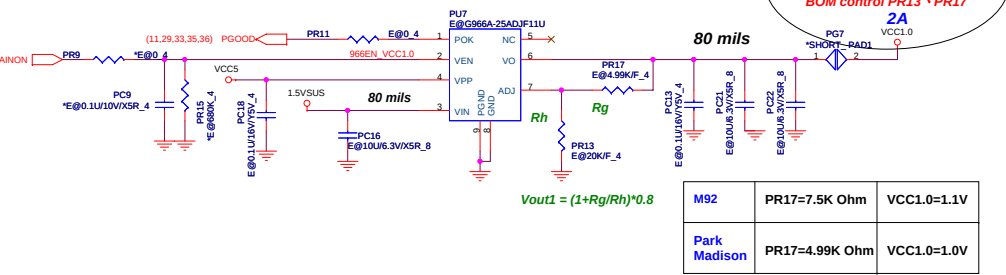
VCC1.8



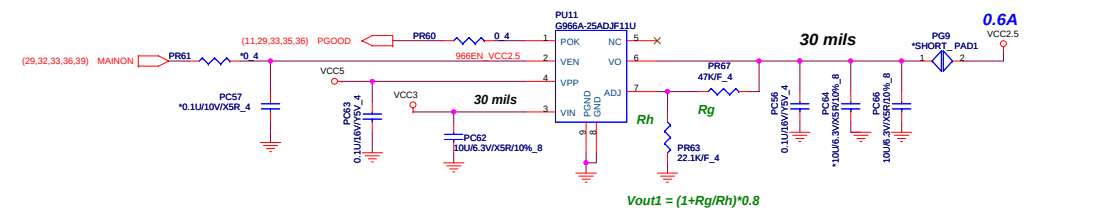
VCC0.9



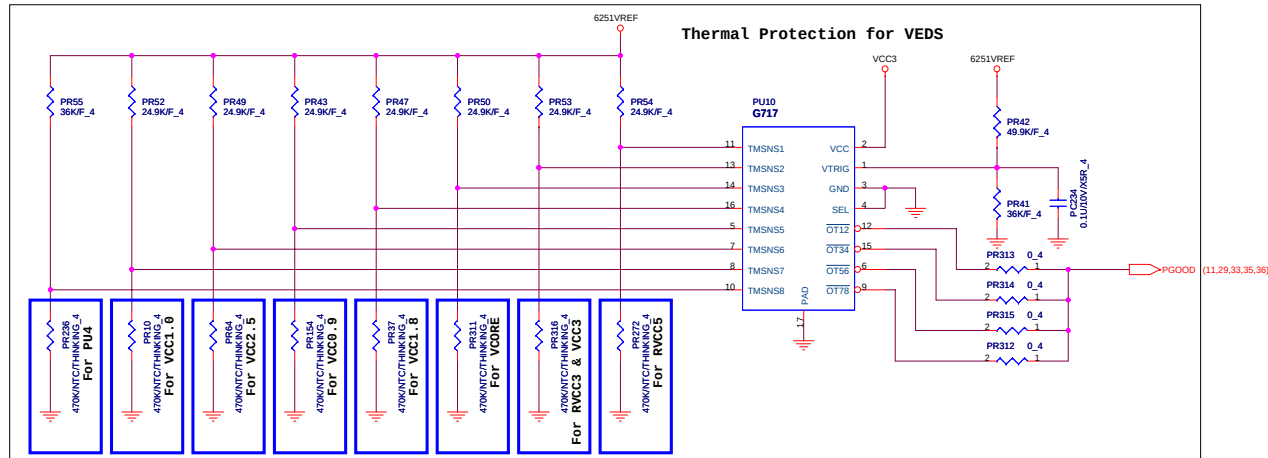
VCC1.0

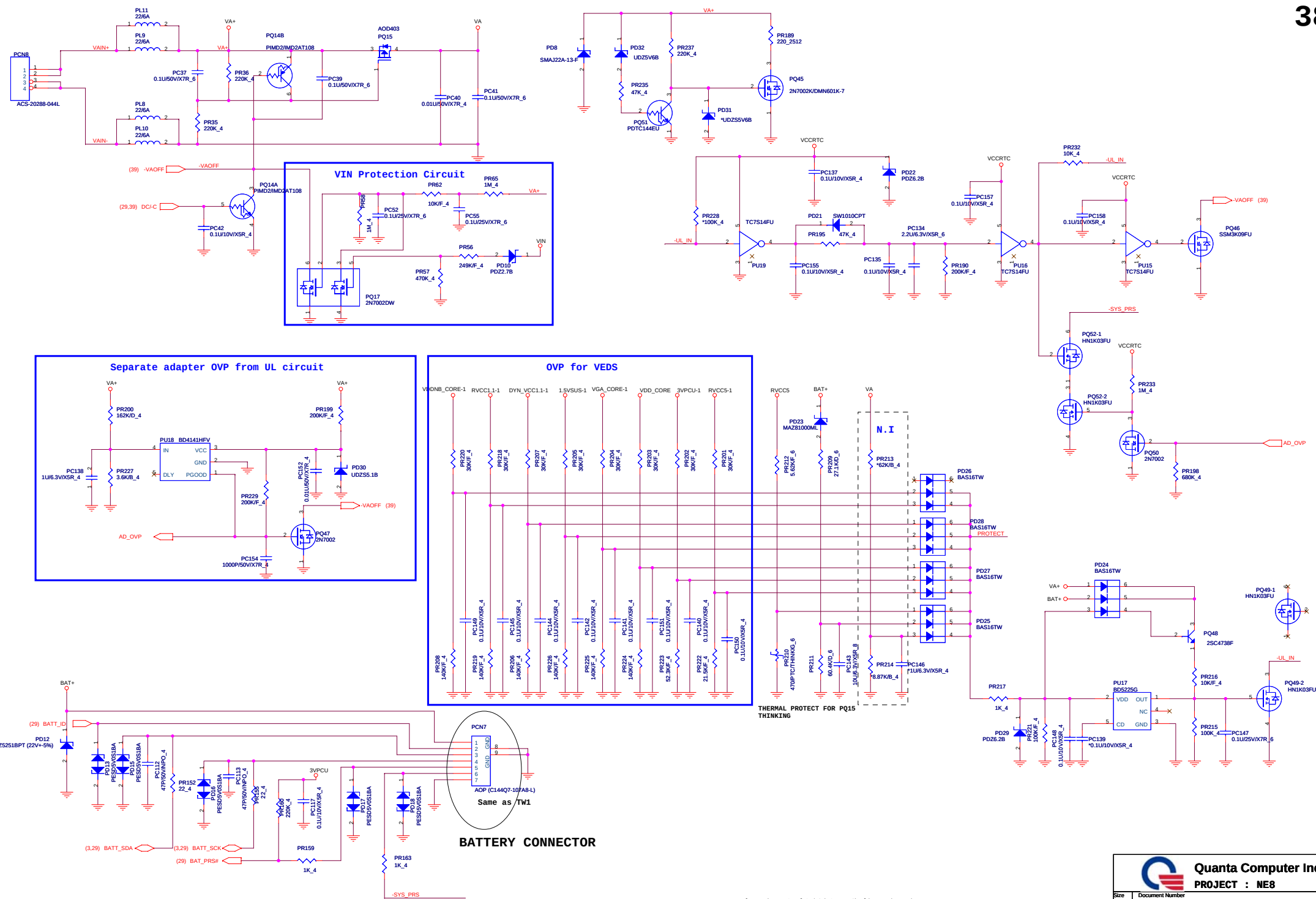


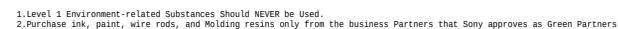
VCC2.5

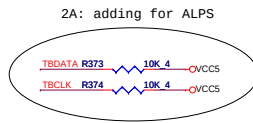
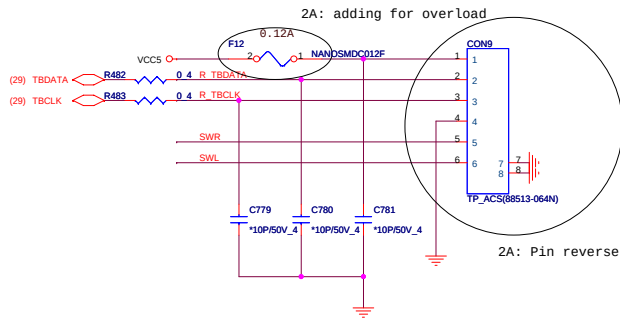
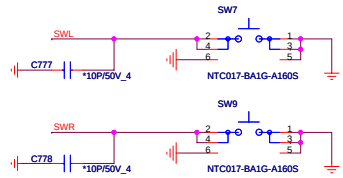


Thermal Protection for VEDS

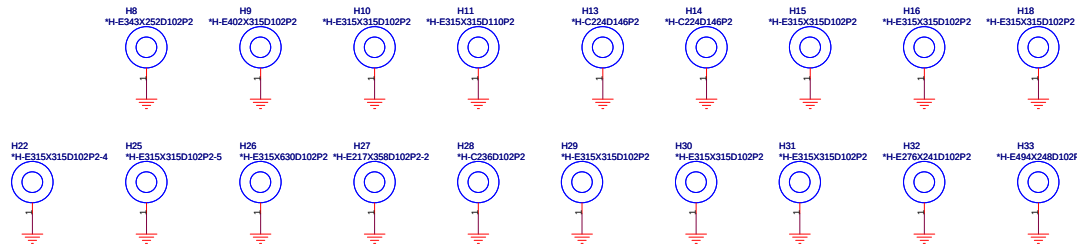






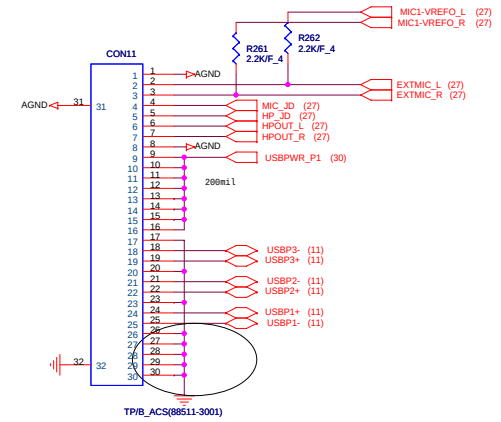
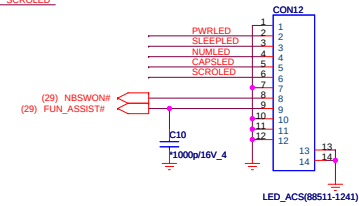
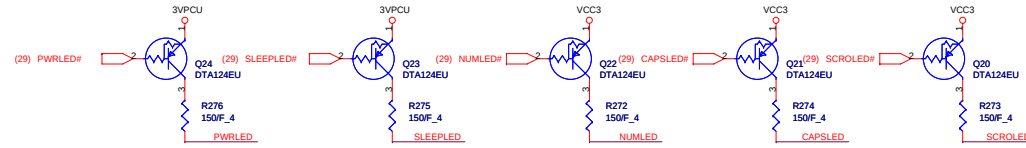
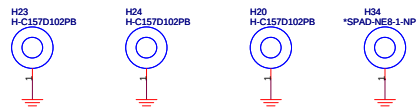


2A: Pin reverse



WLAN

BT

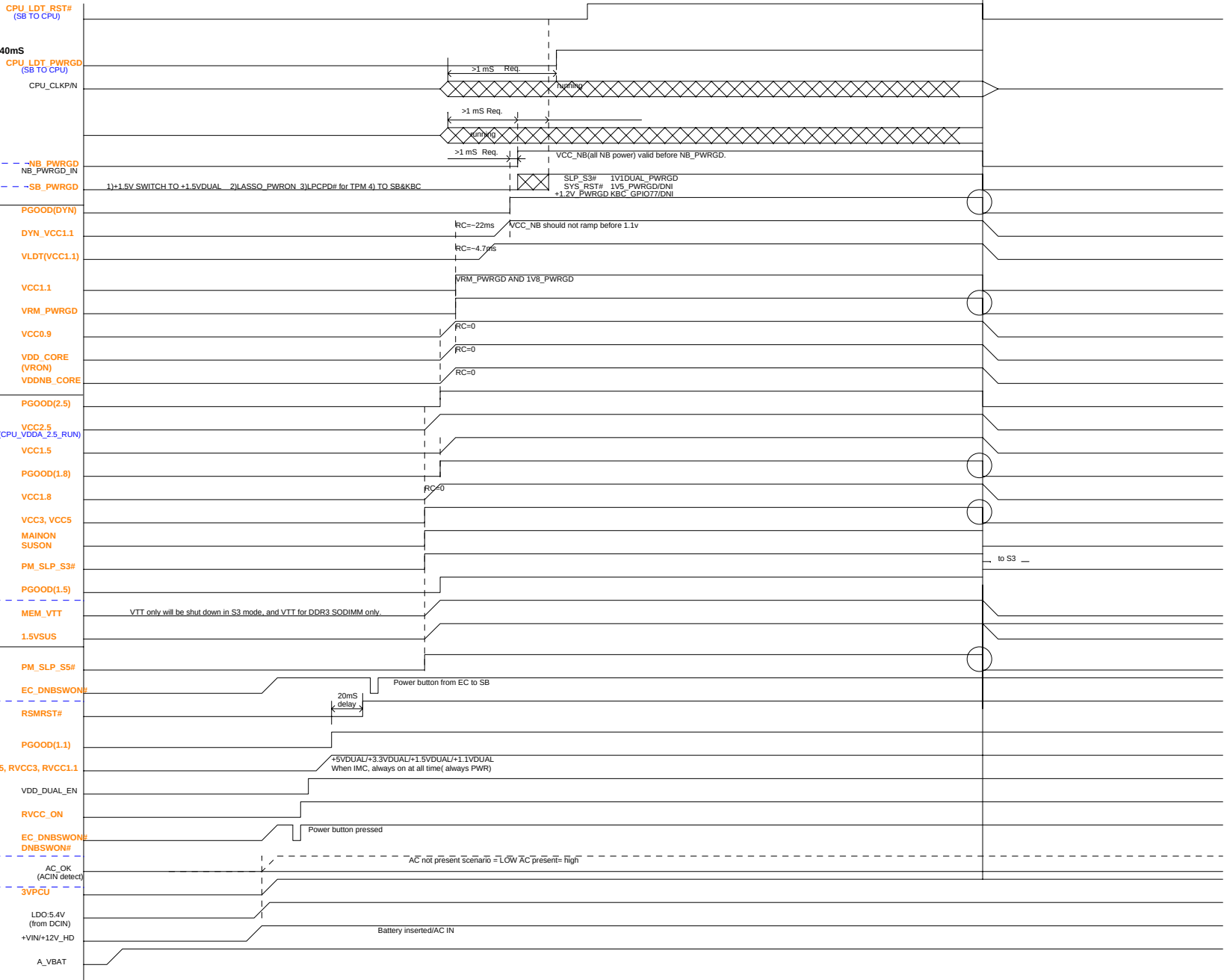
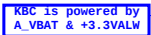
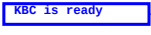


2A: change CON11 form 26pin to 30pin.

SB800:

- 1, +3.3VDUAL ramp before +1.1VDUAL
- 2, +3.3V ramp before +1.8v
- 3, +1.8V ramp before +1.1v
- 4, +3.3v ramp before +1.1v
- 5, +3.3VALW_R ramping down time > 300us
- 6, 50us <= All power rails exceed +3.3VALW_R <= 40ms
- 7, 100us <= +3.3VALW_R <= 40ms

RS880:
 1, $0 < (+3.3V) - (+1.8v) < 2.1$
 2, +1.8V ramp before +1.1v
 3. +1.1V ramp before VCC_NB



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2A Adding R159 (10K) for shut down issue.

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